MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE No. MCB 143

ELLIOTT BROTHERS (LONDON) LTD.,
Mobile Computing Division,
Elstree Way,
Borehamwood,
Hertfordshire

Telephone: ELStree 2040

September, 1966

Whilst every effort is made to ensure accuracy in this Manual, Elliott Brothers (London) Ltd., cannot be held responsible for any errors. Statements made are not to be construed as a specification of the equipments described.

Drawings used in the manual are typical. The machine drawings issued with each computer include the latest applicable modifications and should be used for detail servicing.

INTERPRETATION OF DRAWINGS

Logic symbols used throughout are defined by Fig. A6 (Logic Symbols and Circuits for the MCS 920B Computer).

Certain signal or waveform names are enclosed by square brackets, e.g. [X]. These brackets denote an output available for connection to the Display Unit (Cat. No. MCB. 43 or 44). Similarly, the word "Margin" against a pin number indicates points to which the Marginal Test Unit (Cat. No. MCB. 52) is connected.

Position occupied (within the rack) and board type are quoted on overall logic drawings in the form 57/A-FM. Fig. A3 details all boards in the MCS 920B Computer, together with type and function performed.

Element references take the form of a letter followed by a number ranging from 01 upwards. The letter defines the position occupied by a Logic Sub Assembly (LSA) on a parent, plug-in logic board. The number denotes the type of LSA in that position, e.g. B/01. Identification of element with respect to LSA is shown by the pin numbering.

CONTENTS

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE No. MCB 143

PART 1: CENTRAL PROCESSOR

CHAPTER 1: INTRODUCTION

CHAPTER 1

CONTENTS

APPENDICES

LIST OF FIGURES

CHAPTER 1

1. INTRODUCTION TO MCS 920B SYSTEM

The MCS 920B system is constructed with individual units from a range of catalogue items.

With the exception of paper tape and test equipment, which are standard items, two groups of units are available: military pack (sealed and generally ruggedised) and standard (19 in. rack mounting).

Whilst the available units are described in detail in the appropriate part of the Manual, a list of catalogue items, with optional alternatives, is given below for basic MCS 920B systems.

For convenience, this list is arranged in five groups:

(i) Central Processors

(ii) Ancillary equipment

(iii) Paper tape equipment

(iv) Power supply unit

(v) Test equipment

(i) Central Processors

MCB 1 MCS 920B Computer, 8,192 Word Store, Standard 19 in. rack mounting.

MCB 2 MCS 920B Computer, 8,192 Word Store, Military pack.

MCB 7 MCS 920B Computer, 8,192 Word Store, Similar to MCB 2, but without sealed case and anti-vibration mountings.

With the exception of the core stacks, standard and military versions are similar in design. The military stack is ruggedised and contains heating elements which enable the computer to be more rapidly warmed-up from temperature below -10°C.

MCB.11 Desk fittings. Includes fan, mains filter and remote paper tape control panel for use with MCB.1 in 903 desk.

(ii) Ancillary equipment

MCB.12 Additional 16,384 words store, standard.

MCB.13 Additional 16,384 words store, military.

MCB.46 Additional 8,192 words store, standard.

MCB.47 Additional 8,192 words store, military.

Single or combinations of the above units enable the storage capacity of the computer to be increased in multiples of 8,192 words to a total of 57,344 words of additional storage.

Note: A separate computer power supply unit is required for each additional 32,768 words of storage.

MCB.48 Additional 8,192 words store, with Access Control, standard.

MCB.49 Additional 8,192 words store, with Access Control, military.

This facility provides an additional independent channel into and out of the store to allow information to be transferred autonomously. This channel is identical to the normal channel and may be used by a computer to share common additional store units.

MCB 50 Autonomous Transfer Controller, standard.

MCB 51 Autonomous Transfer Controller, military.

This unit controls autonomous transfer of words to and from additional stores via the access control facility. Words may be transferred to or from one of four input or out channels. The transfers take place without going through the computer registers.

MCB 40 Control Unit, standard

MCB 41 Control Unit, free standing

MCB 45 Control Unit, free standing. Similar to MCB. 41 but in 903 colour scheme.

The Control Unit functions in three modes:

(i) AUTO - The program commences automatically when power is switched on.

(ii) OPERATE - The normal mode used by an operator to control the computer.

(iii) TEST - Engineer's facility for engineering/ programming tests.

MCB 42 Computer Start-Address Plug

This plug may be used in place of a control unit when the computer is to be used on a fixed program; the effect of the plug is to cause the computer automatically to enter the program retained in the store as soon as power is connected to the computer. The plug can be used only when a program has been placed in the store. A control unit or program loading unit is necessary for this.

(iii) Paper Tape equipment:

MCB 60 Paper Tape Controller, standard.

This unit enables the computer to be connected to:

one paper tape reader, 250 ch/sec
Cat. MCB 69, 70

or one paper tape reader, 500 ch/sec
Cat. MCB 71
one paper tape punch, 110 ch/sec
Cat. MCB 74

Paper of up to 8 tracks can be read and punched; necessary manual controls are provided.

MCB 62 Program Loading Unit

An electro-mechanical tape reader with associated logic enabling program tapes to be read into the computer at 20 rows per second. 8 track paper tape punched in either Elliott 503/920 or Elliott 4100/903 format must be used.

MCB 66 Paper Tape and Teleprinter Controller, standard.

Includes paper tape and teleprinter controller, power supply unit, Elliott tape reader, Cat. MCB 70 or MCB 71.
Westrex tape punch Cat. MCB 74 and Teletype model 33 teleprinter.

A plug-in board is available to enable MCB 66 to be used for on-line applications.

MCB 70 Paper Tape reader, 250 ch/sec

MCB 71 Paper Tape reader, 500 ch/sec

Elliott photo-electric reader for use with 5, 6, 7 or 8 track tape (11/16 in. 7/8 in. or 1 in. wide) of any colour. The stopping distance of the tape is less than one sprocket hole pitch under all conditions, so that read instructions may occur at any rate up to the maximum.

MCB 74 Paper Tape punch, 110 ch/sec

Westrex/Teletype BRPE tape punch for use with tapes of up to 8 tracks (1 in. wide) in any colour. (Waterlow grade A1 recommended)

MCB 79 Flexowriter, 16 in. carriage

MCB 80 Flexowriter, 12 in. carriage

Elliott Model P Flexowriters, used for off-line preparation, editing and printing of 8 track paper tape. The Flexowriter includes paper tape reader, electric typewriter with keyboard and tape punch. The maximum operating speed for tape reading, printing and punching is 10 ch/sec. Uses 503/920 tape format.

(iv) Power Supplies

MCB 38 Mains Filter, 400 c/s, standard.

MCB 39 Mains Filter, 50 c/s, standard.

Mains filter and distribution unit for MCS 920B System.

MCB 24 Computer Power Supply, 240V 50 c/s, standard.

Inputs are provided for 100-125V a.c. and 200-250V a.c. 50 or 60 c/s.

The unit provides regulated supplies of +6V, -6V, -16V, +15V and 24V (unstabilised) to the computer or up to four additional 8,192 words stores.

MCB 21 Computer Power Supply, 20-34V d.c. input, military.

This unit provides regulated supplies of +6V, -6V, -16V, -25V, +15V and the input voltage (20-34V d.c.) to the computer or up to four additional 8,192 words stores.

The unit is sealed and can be adapted for 19 in. rack mounting.

Alternative power supply unit for use with 100-125V a.c. and 200-250V a.c. 50 or 60 c/s mains. Cat. No. MCB 24.

MCB 23 Primary Power Supply, 100-125V or 200-250V a.c. 50-60 c/s input, military.

MCB 29 Primary Power Supply, 117V or 200V, 400 c/s 3 Phase input, military.

Contains power unit with two nickel-cadmium batteries, provides an output of 28V d.c. to computer power supply unit MCB 21.

MCB 30 Paper Tape Power Supply, standard.

Designed for use with MCB 60. Input 100-125V or 200-250V a.c. + 10%, 50 c/s $\pm$ 1 c/s.

Provides $\pm$28V d.c. floating, $\pm$10V d.c. 0V and 10V a.c. The latter supply is used for the tape reader lamp. All voltages are isolated from chassis earth.
Alternative power supply, MCB 32.

MCB 32 Paper Tape Power Supply, standard.

Identical to MCB 30 except that it is frequency insensitive and will operate over the frequency range 50 - 60 c/s. The tape reader lamp is supplied by +10V d.c.

(v) Test Equipment

MCB 43 Display Unit, standard, rack mounting.

MCB 44 Display Unit, standard, free standing.

The unit contains a set of neon indicator lamps which display the contents of the computer registers and the state of important control bistables. Used with the control unit, it provides facilities for locating computer faults. Power supplies are obtained from the computer.

MCB 52 Marginal Test Unit, standard, free standing.

This unit provides facilities for checking the performance of the computer under marginal conditions.

Provision is made for varying:

power supplies, store inhibit current, store drive current, main timing loop delay and pulse generator pulse widths.

Fig. A1 is an interconnection diagram, and details units and connectors for the MCS 920B System.

2. THE MCS 920B COMPUTER

2.1 General

The MCS 920B is a mobile general purpose stored data digital computer operating in the parallel mode, especially suitable for real-time on-line computation. It employs a word length of 18 digits in a fixed point binary system and is program compatible with both Elliott MCS 920A and 903 computers.

The central processor comprises a register system, asynchronous timer, control system, control matrix, program priority logic and internal co-incident current store. A block diagram of the computer is given in Fig. A5.

The register system forms the arithmetic unit of the computer and serves additionally to manipulate information during a computation. The registers provide source and destination for output and input information (to and from peripheral devices) also addressing and accessing the store, Fig. A4 refers.

The control system includes program priority logic by which the computer may be caused to operate on one of four levels of priority available. The control matrix contains the built-in micro-program, producing micro-instructions governing the step-by-step operation of the computer in accordance with program requirements.

The store is an 8,192 word magnetic core store operating on the co-incident current principle, with a cycle time of 6 μs. The store holds the program and operands during a computation together with sequence control and modifier registers. The last 12 locations are reserved for a set of permanently available Initial Instructions which facilitate the reading-in of program tapes.

2.2 Construction

2.2.1 Mechanical

(i) The military version, MCB 2:

$$32\,{}^{3}/_{32}" \times 19\,{}^{3}/_{32}" \times 8\,{}^{3}/_{8}"$$

Weight: 98 lb.

The computer is equipped with anti-vibration mounting points enabling the equipment to be used in various attitudes. The case is hermetically sealed, but is equipped with a pressure relief valve which allows equilisation for any changes in atmospheric pressure that may occur during transportation.

Humidity is controlled by two desiccators. The desiccators should be inspected regularly to ensure that their colour is blue. The desiccators turn pink when damp. Inspection can be made via a window aperture in the knurled, desiccator retaining caps.

NOTE: Do not break seal unless a replacement desiccator is being fitted.

(ii) The standard version, MCB 1, mounted on a 19" rack, or desk in an un-sealed case:

$$31\,{}^{1}/_{2}" \times 19" \times 8\,{}^{7}/_{8}$$

Weight: 75 lb.

2.2.2 Electrical

Logic boards of standard size are used throughout the computer, with +6V, 0V and -6V supplier's feeding standard pin numbers.

The 'parent' plug-in board (8" x 5") may hold up to 14 logic sub-assemblies (LSA) on printed circuit boards (2" x $^{7}/_{8}$") which are mounted on the parent board by component wiring. Sleeves on the wiring space the LSA from the parent board printed track. Figure A2 typifies the parent/LSA layout.

The boards are distributed between the registers, control system and store as shown below (Fig. A3 refers).

SYSTEM	NUMBER OF BOARDS	NUMBER OF TYPES USED
REGISTER	18	1
CONTROL	37	31
STORE	22	8

The total number of boards used in the computer is 77. Boards 26 A-FV and 27 A-FU are only supplied with extra store units.

3. INSTRUCTIONS

3.1 Instruction Control

Instructions are normally obeyed in sequence, and are held in the store in locations allocated by the programmer. The Sequence Control Register provides the address of the next instruction and is automatically incremented by one each time an instruction is obeyed, or replaced by a new address in a jump instruction. By this means, successive instructions are taken from successively addressed store locations until the program has been completed.

Four Sequence Control Registers are provided, one for each of the four program priority levels available. The Sequence Control Registers are held in locations 0, 2, 4 and 6 of the store, and relate to program levels 1 to 4 respectively.

Four B-registers (modifier registers) are provided, also held in the store (locations 1, 3, 5 and 7), and correspond to the four program levels. Thus the address of an instruction on any program level may be modified by the addition of the associated B-Register.

NOTE: B-modification will affect the contents of the auxiliary register, as will Functions 0, 2, 7, 9, 11, 12, 13 and 14.

3.2 Number and Instruction Representation

The instruction is normally used to specify the operation to he performed and provides the address of the store location in which one of the two operands necessary may be found. The second operand is located in the accumulator. (Under certain circumstances the latter may be placed in the accumulator and auxiliary register.) Completion of each function either leaves the result in the accumulator (from which an output device may be fed) or places it in the accumulator and auxiliary register or the store.

The computer operates on a fixed-point binary system (although the binary point is not represented physically) in the parallel mode, all digits of a computer word being generated and/or displayed simultaneously. A word length of 18 binary digits is used in which the least significant, numbered 1 is at the right and the most significant, numbered 18, is on the left. In multiplication and division, a 34-bit product or dividend is placed in the accumulator and auxiliary register. The most significant digits of such a number are placed in the accumulator.

When a word represents a number, the 18th digit is used to denote the sign, this indicates whether the number following is positive or negative. Where the sign digit is '0', the following 17 digits constitute a positive number; the converse applies where the sign is '1'. Negative numbers are represented by their complement with respect to two.

An instruction is divided into three groups representing:

the modifier B, 0 or 1; the function F, $0 \leqslant F \leqslant 15$
and the address B, $0 \leqslant N \leqslant 8191$.

3.3 Instruction Code

The full effect of each function is specified in the following list:

A, Q, B, S } Refer to the contents of the { accumulator; Q-register; modifier register; sequence control register

n means the contents of the store location specified by N the modified address of the instruction.

(A, Q) means the double length number held in A and Q.

Subscripts are used to indicate particular bits or a grasp of bits of the number concerned.

Function	Title	Operation	Effect
0	Set B-register	Place in the B-register of the current program level, and in the Q register, the contents of the store location specified by N. The contents of Q are affected by this function.	B: = n Q: = n
1	Add	Add the contents of the store location specified by N to the accumulator. The contents of Q are not affected by this function.	A: = A + n
2	Negate and Add	Negate the contents of the accumulator and add the contents of the store location specified by N The contents of N are also placed in the Q register by this function.	A: = n - A Q: = n
3	Store Auxiliary Register	Place the most significant 17 bits of the Q register in the least significant 17 bits of the store location specified by N. The most significant bit of the store location is made zero.	n_{18}: = 0 $n_{1-17} = Q_{2-18}$

Function	Title	Operation	Effect
3		The contents of A are not affected by this function.	
4	Read	Copy the contents of the store location specified by N into the accumulator.	A: = n
5	Write	Copy the contents of the accumulator into the store locations specified by N.	n: = A
6	Collate	Place ones in the accumulator in only those digit positions in which both the contents of store location N and the contents of the accumulator are ones. (Alt., form in the accumulator the logical product of the contents of the accumulator and of the store location specified by N.)	A: = A & n
7	Jump if zero	If the number in the accumulator is zero, place N in the sequence control register at the current program level. The contents of the Q register are affected by this function.	A1-16: n if A = 0 Q: = B, F, N S17, 18 are not defined.

Function	Title	Operation	Effect
8	Jump	Place N in the sequence control register of the current program level. The contents of A and Q are not affected by this function.	S1-16 = n S17, 18 are not defined.
9	Jump if negative	If the number in the accumulator is negative, place N in the sequence control register of the current program level. The contents of Q are affected by this function.	S1-16: n if A < 0 Q: = B, F, N S17, 18 are not defined.
10	Count in Store	Increment the contents of the Store Location specified by N by $+2^{-17}$. The contents of A and Q are not affected by this function.	n: = n + 2^{-17}
11	STORE SCR.	Copy the 13 least significant digits of the SCR of the current program into the store location specified by N. The 5 most significant	N1-N13 = S1-S13 N14-N18 = 0 Q14, 15, 16 = S14, 15, 16. As S17, 18 are not defined, so Q17,18

Function	Title	Operation	Effect
11		digits of the SCR are placed in Q. The contents of A are not affected by this function.	are not defined.
12	Multiply	Multiply the number in the accumulator by the number in the store location specified by N, and place the result in the accumulator and the most significant 17 digit position of the Q register. The least significant digit if the Q register is made zero.	(A, Q_{2-18}): Axn Q, : = 1 if A < 0 otherwise = 0.
13	Divide	Divide the number in the accumulator and the most significant 17 digits of the Q register by the number in the store location specified by N, and place the results in the accumulator, making the least significant digit a 1.	$A: = \frac{(A, Q_{2-18})}{n} \pm 2^{-17}$ A1: = 1. $Q: = \frac{(A, Q_{2-18})}{n} + 0(-2^{-16})$ Q: = 0

Function	Title	Operation	Effect
14	Shift Block Transfer		
(a)	Left Shift $0 \leqslant N \leqslant 2047$ Bit 13=0, Bit 12=0	Shift the contents of the accumulator and Q register left by the number of places specified by N. (= multiply by 2^N)	$(A, Q) := (A, Q) \times 2^N$
(b)	Right Shift $6144 \leqslant N \leqslant 8191$ Bit 13=1, Bit 12=1	Shift the contents of the accumulator and Q register left by the number of places specified by N. (= divide by 2^{8192-N}).	$(A,Q) := (A,Q) \times 2^{N-8192}$
(c)	Block input $2048 \leqslant N \leqslant 4095$ Bit 13=0, Bit 12=1	Transfer x words of information from the device specified by bits 1-11 of N into Store locations m to y→y + x - 1. y is the contents of the accumulator and x is the contents of the auxiliary register. ($x < 4095$).	Q remains = x A remains = y
(d)	Block output $4096 \leqslant N \leqslant 6143$	Transfer x words of information to the device specified by bits 1 to 11 of N from store locations	Q remains = x A becomes = last information word output to peripheral.

Function	Title	Operation	Effect
14(d)	Bit 13=1, Bit 12=0	y⇒y + x -1, where y = the contents of the accumulator and x = the contents of the Q register. ($x < 4095$)	
15	Input/Output		
(a)	Input $0 \leqslant N \leqslant 2047$	Input to the accumulator One 18 bit word from the device specified by bits 1 to 11 of N.	Q is unaffected by the 15 instructions
(b)	Output $4096 \leqslant N \leqslant 6143$	Output from the accumulator one bit 18 word to the device specified by bits 1 to 11 of N.	
(c)*	Tape reader Input $2048 \leqslant N \leqslant 2063$	Input one character from the tape reader channel. Shift the previous contents of the accumulator left by seven places and place the input character in the least significant seven bit positions on the accumulator.	
(d)	Tape punch Output $6144 \leqslant N \leqslant 6159$	Output the least significant eight bits of the accumulator to the tape punch.	

Function	Title	Operation	Effect
14(e)	Program Terminate N = 7168	Terminate current program level.	
* These instructions may be used for input or output when an on-line teleprinter (Cat. No. MCB 66 is connected).			

NOTE: The 920 Series Instruction Code Summary is given in Appendix 3.

3.4 Initial Instructions

A set of permanently available initial instructions facilitate the reading of program tapes into the computer. These may be used to load a checked program, translation input routine or compiler (920 T.2, S.I.R., ALGOL).

Entry is effected by setting the address key switches of the Control Unit to the starting address 8181 the initial instructions.

NOTE: The last 12 Store locations, i.e. 8180 - 8191 are reserved for the wired-in initial instructions.

The initial instructions, in effect a short program, enable the first three program words to be written into store locations 8177, 8178 and 8179. Control is then transferred to location 8177. Where these program instructions set the B-register to -n and transfer control to location 8182, words may be read into a sequence of n locations terminating at location 8179. Control is next transferred to location 8177 so that a transfer instruction read into that location can trigger the program.

The initial instructions and their respective addresses are tabulated below:

Starting

Address	Instruction			Effect
'N' digits	'B'	'F'	'N'	
8180	/	15	8189	(- 3)
8181		00	8180	(Set B-register to -3)
8182		04	8189	(Set Accumulator initially)
8183		15	2048	(Shift and input tape character)
8184		09	8186	(Jump to 8186 if accumulator is negative)
8185		08	8183	(Jump to 8183 if accumulator is positive)
8186		15	2048	(Shift and input final tape character of word).
8187	/	05	8180	(Store word read-in)
8188		10	0001	(Count in B-register)
8189		04	0001	(Read B-register)
8190		09	8182	(Jump to 8182 if accumulator is negative)
8191		08	8177	(Jump to 8177 if accumulator is positive).

Setting the start address 8181 on the keys of the Control Unit and depressing the 'JUMP' button causes a jump instruction to be given which places 8181 in the Sequence Control Register. The next instruction to be obeyed is thus 00 8180. From the table given above it will be seen that this instruction will cause the B-register to be set with the content of location 8180 which, numerically, is -3. Incrementing the Sequence Control Register on completion of the above will produce the address 8182, hence the next instruction will be 04 8189. This initially sets the accumulator by reading in 0.0100000000000001 to ensure that in the process of shifting which accompanies the reading in of the first two tape characters, the accumulator remains positive.

The programme is designed to disregard blank tape (for these leave the accumulator positive) and detection of program information occurs only when the accumulator is made negative. A condition achieved by preceding each group of three information characters required to construct one 18-digit computer word by a 'marker'. This character (the binary 76) when left shifted to the four most significant digit positions of the accumulator makes this register negative. The micro-program will respond to this condition and permit one further tape character to be read. This results in the 'marker' character going out of range and also the three most significant digits of the first program character read, leaving the accumulator set by the first 18-digit program instruction.

Location 8184 is a jump instruction, testing the accumulator for the negative content; the 'marker' will satisfy this condition when it occupies the four most significant digit positions in the form 1100.

The shifting arrangement necessary when reading paper tapes will be readily understood by reference to Part 1, Chapter 4, Section 24 (Function 15).

Initially, however, the accumulator will be positive, containing 0.000/0000001/1001100; the 'marker' occupying the 7 least significant digit positions. The 'jump if negative' instruction given by 8184 cannot thus be satisfied and the instruction addressed by 8185 will be obeyed. This instruction, 08 8183, places 8183 into the Sequence Control Register and a second tape character is admitted to the accumulator. Simultaneously the character first read (the 'marker') is left shifted into digit positions 8 to 14. Successive to this, the Sequence Control Register will produce the address of the 'jump if negative' instruction, 8184, which again cannot be satisfied. Incrementing the Sequence Control Register produces 8185 which is re-entered to read a third tape character, shifting the two preceding tape characters read a further 7 digit positions to the left. The first 3 digits of the 'marker' will now be caused to overflow making the accumulator negative.

8186 can now be entered and the instruction 15 2048 implemented. This causes a further tape character to be admitted to the accumulator placing the 'marker' entirely out of range and leaving the accumulator set with the first program word - the first three digits of which will also be placed out of range.

The pattern emerging from the above operations can be seen from the following:

(i)	001000000000000001	Accumulator set initially
(ii)	00000000001:1001100	First 7 digit shift. 'Marker' placed in accumulator.
(iii)	0001:1001100: 1st info. ch.	Second 7 digit shift. First information character placed in accumulator.
(iv)	1100:1st info. ch:2nd info. ch.	Third 7 digit shift. Second information character placed in accumulator which is negative by reason of the partially out of range 'marker'.

The initial instructions make provision for storing this first program word when the address 8187 is entered to produce the /05 8180 instruction. The first program word will now be written into the B-modified address 8180. The current content of the B-register is -3, therefore the addition of this to 8180 gives 8177 as the location in which this first word must be written.

The process of incrementing the Sequence Control Register or S.C.R. will now give the address 8188; the instruction therein (10 0001) will count or add $+2^{-17}$ to the B-register, reducing the modifier to -2.

The initial instructions will be automatically re-entered from location 8182 until the B-register becomes positive; the remaining instructions test for this condition. When the B-register is positive the jump instruction relative to address 8191 will place 8177 into the S.C.R. and the next instruction to be obeyed by the computer will be the first program word read. At this point the second and third program words read will occupy store location 8178 and 8179 (by the action of B-modification). Where these program instructions set the B-register to -n and then transfer control to location 8182, words may be read into a sequence of n locations terminating at location 8179. Control is next transferred to location 8177 so that a transfer instruction read into that location can trigger the program.

4. PROGRAM INFORMATION FROM PAPER TAPE

The normal program input medium to the MCS 920B computer is from 8-hole punched tape delivered via an Elliott high speed paper tape reader.

Parity may occupy positions 5 or 8 (modes 1 or 2) or be defined by programs prepared for mode 3 operation of the paper tape

controller. Part 3, Chapters 2 and 3 refer.

Full particulars of the range of programs available are given in the Elliott 903 Program Library and details of programming the MCS 920B Computer in the Elliott MCS 920B Program Manual Cat. No. MCB 144.

5. SYMBOLIC INPUT ROUTINE (S.I.R.)

S.I.R. enables machine code programs to be written with addresses referred to by invented names. It simplifies editing, as the insertion or removal of instructions does not require the wholesale modification of addresses in the remainder of the program. Also it is easier to spot mistakes in names than in numbers.

Store locations must be reserved by the programmers by labelling them with the invented names. The addresses are then allocated to the locations at assembly time, thus removing from the programmer the burden of organising store space.

S.I.R. can output a relocatable binary version on paper tape to be re-input by a loader routine, in addition to assembling programs to be run immediately on a load and go basis. This makes more store space available for the program than with load and go. An important feature is that the loader will link together relocatable binary tapes of separately assembled routines to form one program.

Debugging facilities include trace and check routines, and the ability to make corrections at run time in S.I.R. code. The assembler and loader can also output a listing of names with their allocated addresses.

Full details are given in the Elliott 903 Program Library.

6. ALGOL COMPILER

ALGOL is the international science-orientated computer language that utilizes programs written in a combination of English words and mathematical expressions.

ALGOL produces an object program on paper tape which may subsequently be re-input for execution.

The Elliott 903 ALGOL is distributed as a set of three tapes:

(i) The translator in sum checked binary.

(ii) The interpreter and library combined in sum checked binary.

(iii) The library tape in sum checked relocatable binary.

Full details are given in the Elliott 903 Program Library.

7. TRANSLATION INPUT ROUTINE

The functions of the Translation Input Routine is to read, translate and place in store the programs or other data recorded on punched paper tape in the standard notations used for punching. (Appendix 1 refers. The 903 Telecode is given in Appendix 2.). This includes instructions, integers and fractions.

As an example of the case of this routine, a description of the facilities offered by 920 T2 follows.

The data to be read is punched on tape in accordance with the conventions described below. The tape is placed in the tape reader and 920 T2 is then entered at address 7759.

A group of characters are punched on the tape as a label to identify it. The 920 T2 will copy all data between = and two or more

consecutive blanks and store them from 7700 backwards in the store with two characters per word. When a) is encountered on the tape, the label if any will be output in parity checked 8-hole flexowriter code.

APPENDIX 1

920 Telecode

Character	Numerical Value	B.S. Meaning (Digit pos. 5 and 8 is parity and therefore disregarded).	Elliott (503) Flexowriter action
Zone 0			
00000.000	0		Ignore
00010.001	1		Ignore
00010.010	2	new line	new line
00000.011	3	paper throw	paper throw (if fitted)
00010.100	4	Tabulate	Tabulate
00000.101	5	Backspace	Backspace (if fitted)
00000.110	6	Shift out	Ignore
00010.111	7	Shift in/run out	run out
00011.000	8	(.	(
00001.001	9	)	)
00001.010	10	, ...	,
00011.011	11	£	£
00001.100	12	. . . . .	:
00011.101	13	&	&
00011.110	14	*	*
00001.111	15	/	/
Zone 1			
00110.000	16	0	0
00100.001	17	1	1
00100.010	18	2	2
00110.011	19	3	3
00100.100	20	4	4

Character	Numerical Value	B.S. Meaning	Elliott (503) Flexowriter action
Zone 1			
00110.101	21	5	5
00110.110	22	6	6
00100.111	23	7	7
00101.000	24	8	8
00111.001	25	9	9
00111.010	26	10	10
00101.011	27	11	11
00111.100	28		=
00101.101	29	+	+
00101.110	30	-	-
00111.111	31	.	.
Zone 2			
01010.000	32		;
01000.001	33	A	A
01000.010	34	B	B
01010.011	35	C	C
01000.100	36	D	D
01010.101	37	E	E
01010.110	38	F	F
01000.111	39	G	G
01001.000	40	H	H
01011.001	41	I	I
01011.010	42	J	J
01001.011	43	K	K
01011.100	44	L	L
01001.101	45	M	M
01001.110	46	N	N

Character	Numerical Value	B.S. Meaning	Elliott (503 Flexowriter action
Zone 2			
01011.111	47	O	O
Zone 3			
01100.000	48	P	P
01110.001	49	Q	Q
01110.010	50	R	R
01100.011	51	S	S
01110.100	52	T	T
01100.101	53	U	U
01100.110	54	V	V
01110.111	55	W	W
01111.000	56	X	X
01101.001	57	Y	Y
01101.010	58	Z	Z
01111.011	59		
01101.100	60		
01111.101	61	ARQ (see note 1)	Ignore
01111.110	62	Escape (see note 2)	/ (non escaping)
01101.111	63		
Zone 4			
10010.000	64	Space	Space
10000.001	65	)	
10000.010	66	)	Programatic
10010.011	67	)	(see note 3)
10000.100	68	)	
10010.101	69	)	
10010.110	70	Shift out	Ignore
10000.111	71	Shift in/run out	Ignore

Character	Numerical Value	B.S. Meaning		Elliott (503) Flexowriter action
Zone 4				
10001.000	72		)	
10011.001	73		)	
10011.010	74		)	Programatic
10001.011	75		)	
10011.100	76		.. ..	Halt
10001.101	77		)	
10001.110	78		)	Programatic
10011.111	79		)	
Zone 5				
10100.000	80	0 (Suffix)		
10110.001	81	1 (")		
10110.010	82	2 (")		
10100.011	83	3 (")		
10110.100	84	4 (")		
10100.101	85	5 (")		
10100.110	86	6 (")		
10110.111	87	7 (")		
10111.000	88	8 (")	.. ..	[
10101.001	89	9 (")	.. ..	]
10101.010	90			10 (Suffix)
10111.011	91		.. ..	<
10101.100	92		.. ..	>
10111.101	93		.. ..	↑
10111.110	94		.. ..	~
10101.111	95		.. ..	%

Character	Numerical Value	B.S. Meaning	Elliott (503) Flexowriter action
Zone 6			
11000.000	96		?
11010.001	97	a	a
11010.010	98	b	b
11000.011	99	c	c
11010.100	100	d	d
11000.101	101	e	e
11000.110	102	f	f
11010.111	103	g	g
11011.000	104	h	h
11001.001	105	i	i
11001.010	106	j	j
11011.011	107	k	k
11001.100	108	l	l
11011.101	109	m	m
11011.110	110	n	n
11001.111	111	o	o
Zone 7			
11110.000	112	p	p
11100.001	113	q	q
11100.010	114	r	r
11110.011	115	s	s
11100.100	116	t	t
11110.101	117	u	u
11110.110	118	v	v
11100.111	119	w	w
11101.000	120	x	x
11111.001	121	y	y
11111.010	122	z	z

Character	Numerical Value	B.S. Meaning		Elliott (503) Flexowriter action
Zone 7				
11101.011	123			
11111.100	124			
11101.101	125			
11101.110	126		. . . . .	- (non-escaping see note 2)
11111.111	127	Erase	. . . . .	

Notes

1. A.R.Q. (Code 61) is short for "Automatic Repetition Query", indicating an automatic request for repetition of a message; this code is only relevant to Telegraphy.

2. "Escape" has the special meaning that the next character is to be interpreted in a special way, i.e. is "escaped" from the code. On the Elliott Flexowriter the special meaning is conveyed by a vertical line being superimposed on the character; this is achieved by the "escape" character causing a vertical line to be printed without advancing the carriage after printing. In teleprinter technology a code which does not advance the carriage is referred to as a "non-escaping" code.

3. "Programatic" functions are concerned with the control of auxiliary equipment which may be attached to the Flexowriter.

APPENDIX 2

903 Telecode

Note: This telecode is also used by the NCR-Elliott 4100 system. The paper tape station normally operates in the 8 track input/output mode. The paper tape station can also be adjusted to work in certain other modes, in particular it can operate in the same mode as the Elliott 503 and 920 computers, dropping bit-5, but not performing a hardware parity check.

ISO Code Value	Telecode Character	Value with Parity	SIR Internal Code (octal)
0	blank	0	
1		129	
2		130	
3		3	
4		132	
5		5	
6		6	
7		135	
8		136	
9	Hor. Tab †	9	
10	Line Feed ¶	10	01
11	Ver. Tab †	139	
12		12	
13	Car. Ref. ‡	141	
14		142	
15		15	
16		144	

ISO Code Value	Telecode Character	Value with Parity	SIR Internal Code (octal)
17		17	
18		18	
19		147	
20		20	
21		149	
22		150	
23		23	
24		24	
25		153	
26		154	
27		27	
28		156	
29		29	
30		30	
31		159	
32	Space	160	00
33	1 ¼	33	
34	"	34	02
35	½	163	03
36	$	36	04
37	%	165	05
38	&	166	06
39	' (acute)	39	07
40	(	40	10
41	)	169	11
42	*	170	12

ISO Code Value	Telecode Character	Value with Parity	SIR Internal Code (octal)
43	+	43	13
44	,	172	14
45	-	45	15
46	.	46	16
47	/	175	17
48	0	48	20
49	1	177	21
50	2	178	22
51	3	51	23
52	4	180	24
53	5	53	25
54	6	54	26
55	7	183	27
56	8	184	30
57	9	57	31
58	:	58	32
59	;	187	33
60	<	60	34
61	=	189	35
62	>	190	36
63	10	63	37
64	` (grave)	192	40
65	A	65	41
66	B	66	42
67	C	195	43
68	D	68	44

ISO Code Value	Telecode Character	Value with Parity	SIR Internal Code (octal)
69	E	197	45
70	F	198	46
71	G	71	47
72	H	72	50
73	I	201	51
74	J	202	52
75	K	75	53
76	L	204	54
77	M	77	55
78	N	78	56
79	O	207	57
80	P	80	60
81	Q	209	61
82	R	210	62
83	S	83	63
84	T	212	64
85	U	85	65
86	V	86	66
87	W	215	67
88	X	216	70
89	Y	89	71
90	Z	90	72
91	[	219	73
92	£	92	74
93	]	221	75
94	↑	222	76
95	← ‡	95	77

ISO Code Value	Telecode Character	Value with Parity	SIR Internal Code (octal)
96	@	96	
97	a	225	41
98	b	226	42
99	c	99	43
100	d	228	44
101	e	101	45
102	f	102	46
103	g	231	47
104	h	232	50
105	i	105	51
106	j	106	52
107	k	235	53
108	l	108	54
109	m	237	55
110	n	238	56
111	o	111	57
112	p	240	60
113	q	113	61
114	r	114	62
115	s	243	63
116	t	116	64
117	u	245	65
118	v	246	66
119	w	119	67
120	x	120	70
121	y	249	71
122	z	250	72

ISO Code Value	Telecode Character	Value with Parity	SIR Internal Code (octal)
123		123	
124		252	
125		125	
126		126	
127	erase	255	

† Flexowriter only

¶ New line on Flexowriter

‡ Teletype only

APPENDIX 3

920 Series Instruction Code Summary

Word format

Digit		18	17 16 15 14	13 12 11 10 9 8 7 6 5 4 3 2 1
Significance	number	-1	2^{-1} 2^{-2} 2^{-3} 2^{-4}	2^{-5} 2^{-6} 2^{-7} 2^{-8} 2^{-9} 2^{-10} 2^{-11} 2^{-12} 2^{-13} 2^{-14} 2^{-15} 2^{-16} 2^{-17}
	instruction	B (Modify)	F (Function)	N (Address)

A number is written as a fraction or as an integer with an implicit multiplier of 2^{-17}.

An instruction is written as two integers (F and N) separated by a space; if B = 1 the first integer is preceded by a /.

Registers

A - accumulator register - 18 bits

Q - ancillary register - 18 bits. Digits 2 to 18 of Q (written Q_{2-18}) constitute the auxiliary register which is used as an extension of A to hold double length numbers; Q_{2-18} then have significances 2^{-34} to 2^{-18}.

AQ - refers to the accumulator and auxiliary registers when together holding one number.

S - sequence control register - 16 bits

B - modifier register - 18 bits

Store addressing

The store location referred to by an instruction is generally defined by a 16 bit number M calculated as follows:-

Unmodified instruction (B = 0) $M := S_{14-16} + N$

Modified instruction (B = 1) $M := B + S_{14-16} + N$

B should be such that M_{17} and M_{18} would be zero.

Locations 0 to 7 inclusive should not be addressed except during initial setting up for interrupts.

Locations 8180 to 8191 contain the initial instructions which cannot be overwritten. These instruction words can be used as operands.

Instruction code

The effects of instructions are as given in the table below. Where the affect on 920A differs, the difference is noted.

Where something is listed as "affected", programs must be independent of the actual effect. Addresses outside the permitted ranges listed below must not be used (with the sole exception of addresses 0 to 7 listed above).

Notation

A, Q, S, B, AR, indicate the contents of the registers listed above.

M is used for the store address associated with an instruction as defined above.

Primes are used to indicate the contents of store locations, e.g. M' indicates the contents of location M.

T indicates an 8 bit character read from paper tape or teleprinter.

Suffixes are used to indicate individual bit positions, numbered as above, e.g. A_{1-8} means bits 1 to 8 inclusive of A.

ALGOL symbols and syntax are used, the meanings are generally self-evident. Note the use of := meaning "is replaced by"

Operation	Function	Address range permitted	Effect					
			Accumulator A: =	Anc. register Q: =	Sequence reg. S: =	Modifier reg. B:=	Store	Other
Modify	/	-	-	affected	-	-	-	$M:=B+S_{14-16}+N$
Set B reg.	0	$M \geqslant 8$	-	M'	S + 1	M'	-	Interrupt cannot take place after this instruction
Add	1	$M \geqslant 8$	A + M'	-	S + 1	-	-	-
Negate and Add	2	$M \geqslant 8$	M' - A	M'	S + 1	-	-	-
Store aux.	3	$8179 \geqslant M \geqslant 8$ or $M \geqslant 8192$	-	-	S + 1	-	$M_{1-17}' := Q_{2-18}$ $M_{18}' := 0$	-
Read	4	$M \geqslant 8$	M'	-	S + 1	-	-	-
Write	5	$8179 \geqslant M \geqslant 8$ or $M \geqslant 8192$	-	-	S + 1	-	M' : = A	-
Collate	6	$M \geqslant 8$	A and M'	affected on 920A	S + 1	-	-	-
Jump if zero	7	$M \geqslant 8$	-	affected	if A=0 then M else S+1	-	-	-
Jump	8	$M \geqslant 8$	-	- (affected on 920A)	M	-	-	-
Jump if negative	9	$M \geqslant 8$	-	affected	if A<0 then M else S+1	-	-	-

Operation	Function	Address range permitted	Effect					
			Accumulator A: =	Anc. register Q: =	Sequence reg. S: =	Modifier reg. B:=	Store	Other
Count	10	$8179 \geq M \geq 8$ or $M \geq 8192$	-	-	S + 1	-	$M' := M' + 1$	-
Store S.C.R.	11	$8179 \geq M \geq 8$ or $M \geq 8192$	-	S_{14-16} ($Q_{1-13} := 0$)	S + 1	-	$M' := S_{1-13}$	-
Multiply	12	$M \geq 8$	$AQ := A \times M$ (Q_1 affected)		S + 1	-	-	-
Divide	13	$M \geq 8$	$\frac{AQ}{M} \pm 2^{-17}$ ($A_1 := 1$) See note 1	$(\frac{AQ}{M} - 2^{-17}) \pm 2^{-17}$ ($Q_1 := 0$) (i.e. $Q = A - 2^{-17}$) See note 1	S + 1	-	-	-
Shift left	14	$0 \leq M_{1-13} \leq 47$ M_{14-16} ignored	$(AQ + Q_1 . 2^{-35}) := (AQ + Q_1 . 2^{-35}) 2^M$		S + 1	-	-	-
Block input (not 920A) (see note 2)	14	$2048 \leq M_{1-13} \leq 4095$ (M_{14-16} ignored)	affected	affected	S + 1	-	A' := 1st word (A+1)' := 2nd word ⋮ (A+Q-1)' := Qth word	Input from device selected by M_{1-11}

Operation	Function	Address range permitted	Effect					
			Accumulator A:=	Anc. register Q:=	Sequence reg. S:=	Modifier reg. B:=	Store	Other
Block output (not 920A) (see note 2)	14	$4096 \leqslant M_{1-13} \leqslant 6143$ (M_{14-16} ignored)	affected	affected	S + 1	-	-	Output to device selected by M_{1-11} 1st word := A' 2nd word := (A+1)' 3rd word := (A+2)' . . . Qth word := (A+Q-1)'
Shift right	14	$8144 \leqslant M_{1-13} \leqslant 8191$ (M_{14-16} ignored)	$(AQ+Q_1.2^{-35}) := (AQ+Q_1.2^{-35})$ 2^{8192-M}		S + 1	-	-	-
General word input	15	$0 \leqslant (M_{1-13} \leqslant 2047$ (M_{14-16} ignored)	input word	-	S + 1	-	-	Input from device selected by M_{1-11}
Tape reader input	15	2048 (M_{14-16} ignored)	$A_{9-18} := A_{2-11}$ $A_8 := A_1$ or T_8 $A_{1-7} := T_{1-7}$		S + 1	-	-	-

Operation	Function	Address range permitted	Effect					
			Accumulator A:=	Anc. register Q:=	Sequence reg. S:=	Modifier reg. B:=	Store	Other
Teleprinter input (not 920A)	15	2052 (M_{14-16} ignored)	$A_{9-18} := A_{2-11}$ $A_8 := A_1$ or T_8 $A_{1-7} := T_{1-7}$	-	S + 1	-	-	-
General word output	15	$4096 \leqslant M_{1-13} \leqslant 6143$ (M_{14-16} ignored)	-	-	S + 1	-	-	Output to device selected by M_{1-11} Output word := A
Tape punch output	15	6144 (M_{14-16} ignored)	-	-	S + 1	-	-	A_{1-8} output to tape punch
Teleprinter output (not 920A)	15	6148 (M_{14-16} ignored)	-	-	S + 1	-	-	A_{1-8} output to tele-printer
Terminate	15	7168 (M_{14-16} ignored)	-	-	S + 1 (terminated program) 2', 4' or 6' (resumed program)	- 3', 5' or 7' (resumed program)	-	Highest priority program resumed
Interrupt (immediate effect)	-	-	-	-	0', 2' or 4' (entered program)	1', 3' or 5' (entered program)	-	-
Interrupt (effect when resumed)	-	-	-	Q_1 only affected	-	-	depends on interrupt program	-

Note 1 - Division

It is not in general possible to say when the result in A is greater or less than the true quotient. If, however, the quotient can be expressed exactly in 17 or fewer bits counting from the sign digit then the following holds.

(a) Divisor positive. The correct quotient is in Q;
A contains the correct quotient plus 2^{-17}.

(b) Divisor negative. The correct quotient is A $+2^{-17}$;
The contents of Q are the correct quotient less 2^{-16}.

Note 2 - Block input and output

Any block input or output instruction must be immediately preceded by a 0 instruction setting the number of words to be transferred in Q.

Interrupt programs

Programs entered as a result of interrupts must commence and end with the following sequences of instructions.

Entry	5	x_1	-	store accumulator of interrupted program
	3	x_2	-	" A.R. " " "
	.			
	.			
	.			
	.			
Exit	0	x_2)		
		)	-	replace A.R. of interrupted program
	14	1)		
		)		
	4	x_1	-	replace accumulator of interrupted program
	15	7168	-	resume interrupted program

Such a program will be re-entered subsequently at the location following the 15 7168 instruction.

APPENDIX 4

Function Times

The time required to carry out an instruction comprises two parts. Firstly the time required to augment the sequence control register and extract the instruction from the store, and if required, modify the instruction. These times are constant for all functions. Secondly the time required to implement the instruction, which varies from one instruction to another. The following is a list of typical function times:-

Typical Function times

Function		* Typical time (μSec.)	Max. Time (μSec.)
		* for information	
0	Set B-Register	28.5	33
1	Add	24.0	26
2	Negate and Add	27.0	29
3	Store Auxiliary Registers	23.5	27.5
4	Read	24.0	26
5	Write	23.5	27.5
6	Collate	23.5	26
	Jump if Zero		
7	A = 0	26.5	31
	A > 0	21.5	23.5
	A < 0	20.0	22
8	Jump	24.0	26.5
9	Jump if Negative		
	A < 0	26.0	29
	A ⩾ 0	20.0	22

Function		* Typical time (μSec.)	Max. Time (μSec.)
		* for information	
10	Count in Store	24.0	26.5
11	Store S.C.R.	31.6	34.6
12	Multiply	76.5	84
13	Divide	79.5	87.5
14	Shift	22 + 3n n = no. of places shifted	24 + 3.3n
	Block transfer	23.5 + (9.5 + y)x y = device busy	26 + (10.5 + y)x x = no. of words transferred
15	Program terminate	20.5	22.5
	Output	20.5 + y y = device busy time	22.5 + y
	Input	20.5 + y	22.5 + y
	Instruction modification	6.5	7.0

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE No. MCB 143

PART 1: CENTRAL PROCESSOR

CHAPTER 2: LOGIC ELEMENTS

CHAPTER 2

LOGIC ELEMENTS

CONTENTS

LIST OF FIGURES

CHAPTER 2

LOGIC ELEMENTS

1. INTRODUCTION

The logic of the MCS 920 Computer is based on the NAND gate. The logic circuits are assembled on printed circuit boards to form the LSA logic elements as depicted in Fig. A6. Silicon planar epitaxial type transistors are used to give rapid switching time with the saturating logic of 30 ns or less.

2. TYPICAL NAND LOGIC

2.1 The Logic Function

The logical AND function is such that the output is only positive when all inputs are positive together. With an inverted output, the element assumes a NAND function. In the NAND gate logic, the output stage of each element is a switching transistor which presents a high impedance to the next stage when cut-off, referred to as logic 1 and a low impedance when saturated, referred to as logic O. The voltage waveform at the output is therefore determined more by the load impedance than by the driving circuit itself. The NAND logic element performs an inverted AND function to as many as 4 inputs.

The input impedance of the basic NAND gate is 2.2 kΩ and diode to +6V d.c. This is defined as one logic load; Fig. A.6, sheet 2 refers. The inputs and outputs of any element are expressed in terms of these logic loads which are annotated on sheets 2, 3 and 4 of Fig. A.6. If an element is driving several other elements, the input resistances of the driven elements are effectively in parallel.

Transistor characteristics change with temperature, therefore the number of unit loads that can be driven also varies, Fig. A.6 refers.

3. THE NAND CIRCUIT

3.1 The NAND Gate

The basic NAND gate logic circuit configuration with as many as four inputs will have an output of logic 0, when all inputs are at 1. If any input is at logic 0, the output will be at logic 1.

In a NAND circuit, forward saturation bias is established by a voltage source. The bias value is chosen so that saturating current continues to flow if any one input pulse is applied, and transient pulses are required at all inputs to turn off the transistor.

In circuits where semiconductor diodes are used at the gate input, large noise spikes present at the input do not get past the diodes. Also in certain circuit configurations the presence of the diodes will improve the transient response.

4. THE BISTABLES

4.1 General

A bistable circuit results from the series connection of two gated elements with feedback from the output of the added element returned to the input of the original gate. The bistable has two stable states and it can be made to change its state on the incidence of a triggering pulse. The bistable is triggered from one stable state to the other by an external pulse and a second reset trigger pulse is required to switch it back to its original state.

The true and false states are defined in that a 1 or true state is the result of a greater than +2V at the output and a 0 or false state less than 1V.

Each register is an assembly of bistable elements as listed in the following table:-

TABLE 1

Unit	Number of Bistables
G-Register	18
A-Register	18
Q-Register	18
M-Register	18
J-Register	16
P-Register	13
I-Register	4
Process Counter	12
The Overflow Unit	2

4.2 Temporary Storage

In the MCS 920B Computer, LSA elements are arranged in two different types of relaxation circuit for use as temporary storage in registers and various control functions:

(i) Bistable Elements

(ii) Staticizers

4.2.1 The Bistable

The bistable element consists of two LSA elements connected as shown in Fig. C so that the output of one feeds the input of the other. Element A must be an LSA 05 or 06.

The bistable is set with a logic 1 level at inputs X and Y. Two inputs are used so that one can be used for data and the other for

gating the data into the bistable. If the inputs at X and Y are both at logic 1, the output of element A will be at logic 0 and hence the output of element B will be at logic 1. The output from B is fed back to the input of A. Z is normally at logic 1, so that the output of A will remain at logic 0 even though X and Y are no longer at logic 1. The bistable is in the logic 1 stable state with true output from element B and bar output from element A.

The bistable is reset by taking input Z to logic level 0. This removes the hold input at element A, and the bistable is reset.

4.2.2 The Staticizer

Staticizers are used in many control functions and in their simplest form are two LSA 01 elements connected in a feedback pattern of symmetrical design so that the outputs of both feed back into the inputs of the adjacent element, Fig. D refers.

Changes of state are always caused by a logic level 0 at the input. The staticizer may also have its state changed by driving its output to a logic 0 using another element in parallel. This form is not considered in this explanation.

Under quiescent conditions, inputs X and Y are at logic 1 level, one of the outputs of elements A and B will be at logic 1 and the other at logic 0.

If input X goes to logic 0, output A will go to logic 1, the output of B will go to logic 0 and the output of A will remain at logic 1 level even if the input X is returned to a logic 1. If the staticizer was previously in that state nothing occurs.

To reset the staticizer input Y is set to logic 0, the output of element B goes to logic 1 and the output of element A to logic 0.

If the inputs X and Y are set to logic 0 simultaneously, the outputs A and B will both be at logic 1. This is the essential difference between the staticizer and the bistable.

The two outputs of the bistable are the logic inverse of each other.

5. THE LOGIC SUB-ASSEMBLY (LSA)

5.1 LSA 01 Two-Input NAND Gates

The schematic of the two-input NAND gate is depicted in Fig. A6 (LSA 01). It comprises two paralleled input diodes, two resistors and two series diodes in the base circuit of the single transistor.

If both inputs are at 1, diodes D1 and D2 will be non-conducting as they are reverse-biased. If an input is changed to a 0 that input diode will conduct and current will flow via R2 from the +6V supply. This will result in an immediate drop in potential (to approximately +1V d.c.) at the common point of the input diodes.

Resistor R1 will maintain a current of approximately 0.3 mA through the base circuit diodes and resistor R2, resulting in a potential of -0.5V approximately at the base of transistor VT.1. The transistor is completely switched-off with its output at logic 1 appearing as a high impedance to the following stage.

5.2 LSA 02. Three-Input NAND Gates

The schematic of the three-input NAND gate is given in Fig. A6 (LSA 02). It comprises three paralleled input diodes, two resistors and two series diodes in the base circuit of a single transistor.

The circuit operates precisely as LSA.01 with the addition of an extra input diode.

5.3 LSA 03. Four-Input NAND Gate + 2 Inverters

The schematic in Fig. A6 (LSA 03) comprises four paralleled input diodes, two resistors and two series diodes in the base circuit of a single transistor. Two inverter circuits are included on the LSA.

The four input NAND gate operates precisely as that of LSA 01 described in paragraph 5.1 with the addition of a further two input diodes.

5.4 LSA 04. Control Matrix Waveform Amplifiers

The schematic in Fig. A6 (LSA 04) is that of three input high noise threshold matrix amplifiers.

This amplifier is used solely to buffer the output of each matrix diode. Both the circuit of the LSA 04 and its operations are similar to the NAND-gate. Resistor R1 is increased to limit the current flowing in any output of the diode matrix to 0.6 of a logic load. An extra diode is inserted in the base circuit to match the output of the matrix line which is 0.9V at logic 0.

5.5 LSA 05. Triple AND/NOR Gate

The circuit in Fig. A6 (LSA 05) is that of a two-input AND/NOR configuration.

The input diodes D1, D2, D3, D4, D5 and D6 comprise AND gates. Diodes D7, D8, D9, D10, D11 and D12 and the transistor comprise a NOR element.

This element totals three pairs of inputs (LSA 05) the output of each pair being mixed, then inverted by the transistor. The circuit of any pair of inputs is identical to that of the NAND-gate input circuit, consequently the loading rules for the element are also the same as for the NAND-gate.

5.6 LSA 06. Dual AND/NOR gate + NAND gate

The circuit in Fig. A6 (LSA 06) is that of a two-input AND/NOR configuration and a dual input NAND gate.

5.7 LSA 07. 13 Pulse Generators (100 ns and 330 ns)

The circuit in Fig. A6 (LSA 07, 13) is that of two similar types of Pulse Generator, differing only in the capacitance values of C1 and C2 to give different pulse lengths.

Considering the circuit of VT1, the pulse generator comprises a two-input diode gate D1, D2 connected through a capacitor C1 to the base of a transistor. Diodes D3 and D4 are connected together at their inputs to a reference potential of +2.4V d.c.

When both logic inputs are at logic 1, the input diodes are reverse-biased and capacitor C1 is charged through the 2.7K resistor to a potential of approximately +3V. If either one or both logic inputs are switched to a logic 0, the leading edge of the resultant waveform causes a fall in potential at the common input point to approximately +1 volt. This change of potential will be transmitted by capacitor C1 switching off the transistor. The output of the element is now at logic 1.

With a steady state logic 0 at the input and no further rate of change of potential applied to C1, the capacitor will commence to recharge through R3. When the potential at the base of the transistor has

risen to approximately +0.7V, the transistor will switch-on appearing as a low impedance (logic 0) to the next stage. The length of the output pulse is therefore dependent on the time constant of C1 - R3, and the level of the reference voltage. It is independent of the length of the input pulse, the only stipulations necessary being that all logic inputs must be at logic 1 for greater than half the time of the pulse width.

The time constant of C1 - R3 (and C2 - R4) is so arranged, in conjunction with the potential of the effective charging voltage and the reference voltage, to give an output pulse length in nanoseconds equalling the capacitance of C1 in picofarads.

5.8 LSA 08. Voltage Reference (for pulse generators)

The schematic of the Voltage Reference Generator is given in Fig. A6 (LSA 08).

The voltage reference generator comprises two transistors VT1 and VT2, voltage dropping resistors R1 and R3, bias resistor R2, decoupling capacitor C1 and regulating capacitor C2.

LSA 08 is used as a +2.4V reference supply to pulse generators 07, 09, 13 and 14. Input pin 6 is disconnected except when margin testing. The input to the base of VT2 is the potential of the centre tap of series resistors R1 and R2. C1 charges up to peak through R1 (+1V approximately) maintaining a steady bias at the base of VT2. C2 charges to the peak of +2.4V at pin 11 at the emitter of VT1, helping to maintain a steady +2.4V output.

5.9 LSA 09, 14. Pulse Generator

The Pulse Generator LSA 09, 14, is depicted in Fig. A6 (LSA 09). With the exception of the capacitance value of C1, the circuit operation is identical to that of LSA 07, 13.

5.10 LSA 11 Cable Transmitters

The schematic of the Cable Transmitter is given in Fig. A6 (LSA 11). This unit is always used preceding a LSA 12.

The logic elements so far described are not suitable for driving signals along cables for more than very short distances. Where longer paths are unavoidable, special elements are needed to transmit and receive the signals. Their input and output impedances are suitably matched to minimise ringing in the transmission paths.

Transmitter elements used to drive signals along cables of up to 20 ft in length are standard one-input NAND-gates with the output modified by R.3 (470 ohms) to provide a voltage drive for cables.

To reduce power requirements to an acceptable level, only one cable and cable receiver may be connected to each transmitter. The output voltage of the transmitter is controlled by the resistive network formed by the collector resistor (R3) of the transmitter and the input resistor of the receiver to which it is connected. These hold the cable voltage at approximately +3.0V when the transmitter is cut off and at approximately +0.3V when the transmitter is conducting.

5.11 LSA 12. Cable Receivers

The schematic of the LSA 12 Cable Receivers is depicted in Fig. A6 (LSA 12). These units are used following LSA 11.

The LSA 12 Cable Receiver is a single input inverter with series diodes on its input to increase its threshold to approximately +2V. When used with an LSA 11, there is no phase inversion from the input to the output of the pair. With the input at logic 0 the potential at the input to the element is approximately +0.3V. Therefore the potential

at the base of the transistor is approximately -1V, switching-off the transistor to give a logic 1 at its output. If the output of a previous stage is switched to a logic 1, then the potential of the input is approximately +3.0V which initiates a change of potential at the base of the transistor, switching it on. The element thus appears as a low impedance (logic 0) to the next stage. The base input resistor of 220Ω limits the input current, whilst the 22K ensures the transistor base can be reverse-biased.

5.12 LSA 15. Two-Input NAND Gate + 2 Inverting Drivers

The two-input NAND + 2 Inverting Drivers is depicted in Fig. A6 (LSA 15).

The two inverting drivers consist of a simple transistor switch operating in a similar manner to a single input NAND gate. The LSA 15 inverting drivers will drive a total of 14 logic loads because of the low value resistor (R1) used, but also places about 2.2 logic loads on the previous stage. To improve the switching time and to provide a greater voltage swing at the transistor output, a pull-up resistor (R3) is connected to the output of the stage to make it suitable for gating 100 ns pulses into registers.

The two-input NAND gate depicted in the schematic is identical with the two input NAND gate of LSA 01.

5.13 LSA 16. F-Minilog Drivers

The schematic of the F-Minilog Drivers is given in Fig. A6 (LSA 16). The circuit of the F-Minilog Drivers is identical to that of LSA.11 (Cable Transmitters) with the exception that the +6V pull-up resistor to the output collectors of LSA 11 is 470Ω while that of LSA 16 is 1.5K.

The circuit shown in LSA 16 is used solely in the paper tape logic and is used to drive an F-Minilog element of the paper tape logic. Its input circuit is identical to the NAND gate, loading the output of the previous stage with one logic load.

5.14 LSA 17 Paper Tape Receiver

The schematic of the Paper Tape Receiver is given in Fig. A6 (LSA 17). The LSA 17 is used only in the paper tape equipment following an LSA 11 unit.

The LSA 17 and LSA 12 units are similar with the exceptions that in LSA 17, resistor R4 (2.7K) in the +6V power supply has been added enabling it to drive a logic element in the paper tape equipment.

5.15 LSA 18 Single Input Noise Rejection Inverter

This element (LSA 18) is only used on the output circuit of the key-type switches of the computer control unit to reduce the effects of contact bounce, etc. When the input to the element is at logic 1, capacitor C_1 charges through R2. As the charging potential across C_1 rises, the current shunted through the base circuit diodes of the transistor increases until it is switched-on. The output of the element is then a logic 0.

The incidence of a logic 0 to the input capacitor C_1 will short-circuit it and the resulting discharge will pull the potential at the base of the transistor down to approximately -1V, sufficient to turn it off and switch the output of the element to a logic 1. If the switch is closed (to switch to logic 0) and momentarily bounces open, the capacitor will have insufficient time to charge to a level affecting the output of the element.

Any transients resulting from contact bounce at the switch connected to the input of the element, will be absorbed by the network C1-R2 which has a time constant of 1 millisecond.

5.16 LSA 19, LSA 20, LSA 21, LSA 24 and LSA 25. Delayed Start Elements

The Delayed Start Element is constructed from a LSA 19 and one of the group LSA 20, 21, 24 or 25. The combination used depending upon the required time delay.

The circuit elements of LSA's 20, 21, 24 or 25 are chosen so that the delay time is 10 ms per micro-farad of capacitance of C1 and C2. Delay time can therefore be controlled by variation of this capacitance. These LSA's are identical except for the omission of C2 in LSA 21. These LSA's are coupled to LSA 19 which provides the output stage.

Under quiescent conditions the input at pin 2 is at logic 1, which makes the input diode reverse-biased. Transistor VT1 is of the p.n.p. type, so that with the input diode reverse-biased and the base potential of VT1 held at +3V, transistor VT1 is switched-on. The collector current of VT1 is sufficient to switch-on VT2, the output impedance of which will be sufficiently low to short circuit capacitor C1. The collector current of VT2 flowing (via pin 13 to pin 6 of LSA 19) through R5, R6 and R7, D2 and R9 drops the potential at the base of VT3, to approximately -1.3V, sufficient to switch this transistor off and switch transistor VT4 on. Therefore in the quiescent state, the element has a logic 1 at the input, producing a logic 0 at the output.

When the input is switched to a logic 0, a low impedance is seen at D.1, resulting in reverse-biasing of emitter and base; the

collector of VT1 will drop to nearly -6V, switching-off VT2. Capacitor C1 will charge up through R5, R6 and R7 D2 (which is used to improve switch-on time) and R9. As the charging otential across C1 rises the potential at the base of VT3 al o rises, until ıt is high enough to switch-on. The collector/emitter potential of VT3 is then at approximately +0.2V which also holds the potential of the base of VT4 at +0.2V, switching-off this transistor. Consequently the output of the element will switch to logic 1, with a small delay whilst C1 is discharged by VT2.

5.17 LSA 22 Two-Input Transmitters

The Two-input Transmitter is depicted in Fig. A6 (LSA 22) and comprises three dual input AND gates in non inverting buffer stages. The LSA 22 is used preceding LSA 23.

5.18 LSA 23 Gated Receivers

The schematic of the Gated Receiver is given in Fig. A6 (LSA 23). The element comprises three individual receivers.

The input waveforms incident to each receiver are:-

(i) Data Information

(ii) The Gating waveform

With a logic 0 on the data input (pin 2 of VT1 circuit), the transistor is at high impedance and there is no current flow through the transistor. The data waveforms ıncident at the junction of the 820Ω and 470Ω resistors are therefore held. A negative gating pulse to the emitter (pins 1, 3 or 5) of the transistor starts conduction. The input diodes are used to reduce the effect of noise signals by producing a higher threshold.

The LSA 23 is used following LSA 22 and with LSA 28.

5.19 LSA 28 Two Input NAND Gates

The schematic of the Two-input NAND gate is given in Fig. A6 (LSA 28). The element comprises three dual-input NAND gate. The LSA 28 is used as a selection driver for LSA 23.

6. ADDITIONAL LOGIC COMPONENTS

6.1 Semiconductor Diodes

All diodes used in the 920B are silicon planar PN junction type and accomplish a variety of functions that include High-Speed Switching, Logic Gating, Biasing, DC Stabilisation, Temperature Sensing, etc.

The use of diodes in the computer logic circuits is essential in the logic design, if a high performance with minimum number of components is to be achieved. The essential features of the diodes used in the 920B are:

(i) Low forward resistance.

(ii) A typical forward volt drop of 0.6V.

(iii) A very high back resistance with leakage current less than 1 μA.

(iv) Low capacity.

(v) High reliability.

6.2 Zener Diode Voltage Stabilization

Voltage Reference or Zener diodes are silicon rectifiers in which the reverse current remains small until the breakdown voltage is reached then increases rapidly with little further increase in voltage. The breakdown voltage depends upon the diode material and construction which can be varied from 3 to several hundred volts. They can be made

with various power ratings depending on the junction area and the method of cooling.

The working voltage of a Zener Diode is a function of both current and junction temperature. A stabilized supply can deliver a constant output voltage with varying input voltage and output load. The sharp voltage breakdown characteristic of voltage reference diodes makes them useful as stabilizing devices and as voltage reference sources.

6.3 The Silicon Controlled Rectifier (SCR)

The Silicon Controlled Rectifier or thyristor is a high power bistable switching device analogous to a thyratron or ignitron, but with fast switching times and extreme triggering sensitivity.

The SCR is a composite of three PN junctions (PNPN) in one wafer interrelated so that controlled switching is possible.

For more details of operation refer to section on A-GZ board (Part 1, Chapter 5).

6.4 Indicators (Control Unit) Cat. No. MCB. 40

The pushbutton switches on the Control Unit are illuminated by 6V indicator lamps which are controlled by individual lamp drivers.

The lamp driver circuit includes two transistors VT1 and VT2, a single capacitor C5, a diode D4 and two resistors R6 and R43, with supply voltages of +6V d.c., -6V d.c. and 0V. The circuit diagram is given in Fig. A.

The capacitor C5 prevents any noise voltage from switching VT1. If the input to VT1 is low (less than 0.5V) VT1 will be switched-off. VT2 will then be switched-on as it derives its base drive via R6 and D4. The collector of VT2 is connected to a lamp and the lamp will

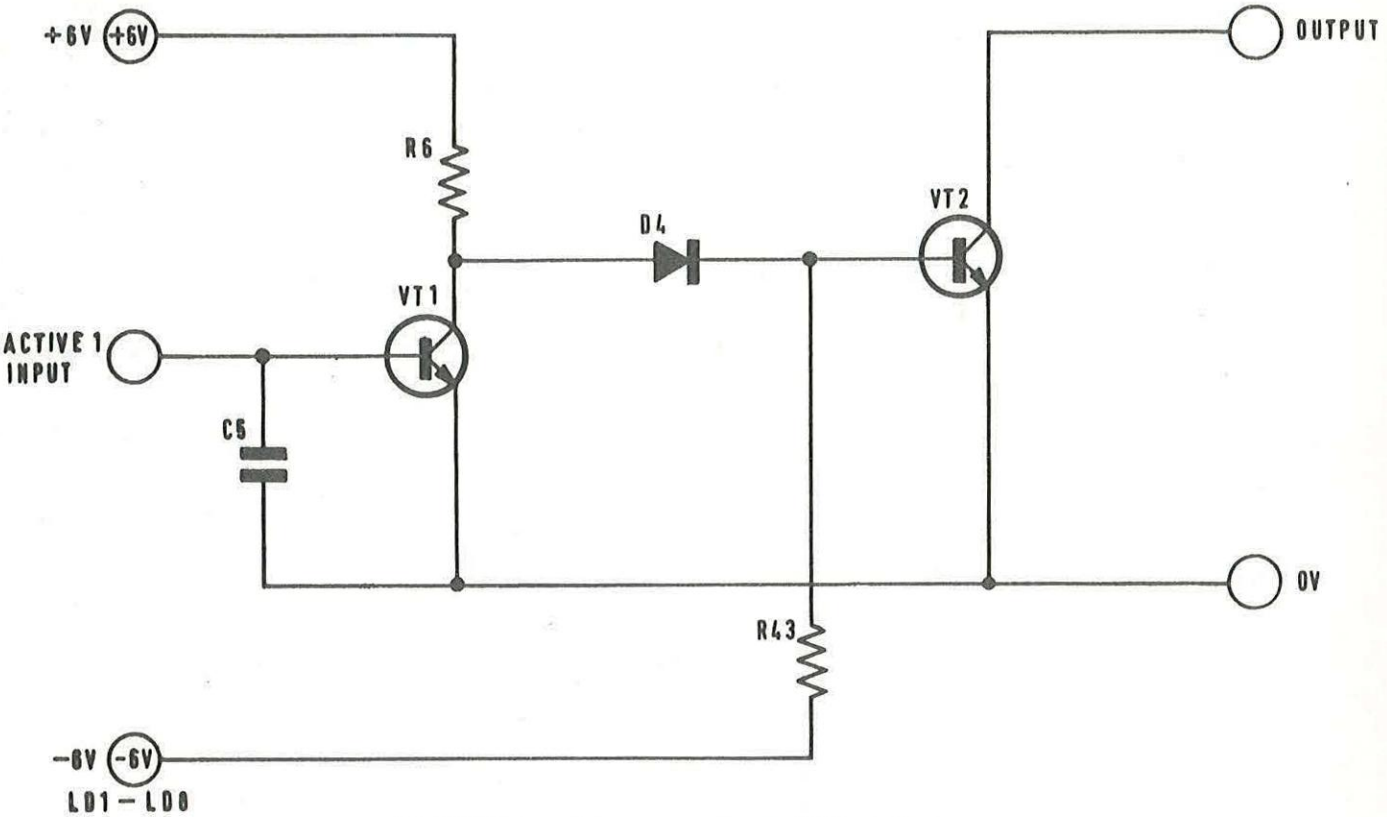
light. If the input to VT2 is high (greater than 1.0V) VT1 will switch on, the collector of VT1 will go to less than 0.3V. VT2 will switch off as its base will be reverse-biased due to the potential drop of the forward biased diode D4.

6.5 Indicators (Display Unit) Cat. No. MCB 43 and 44

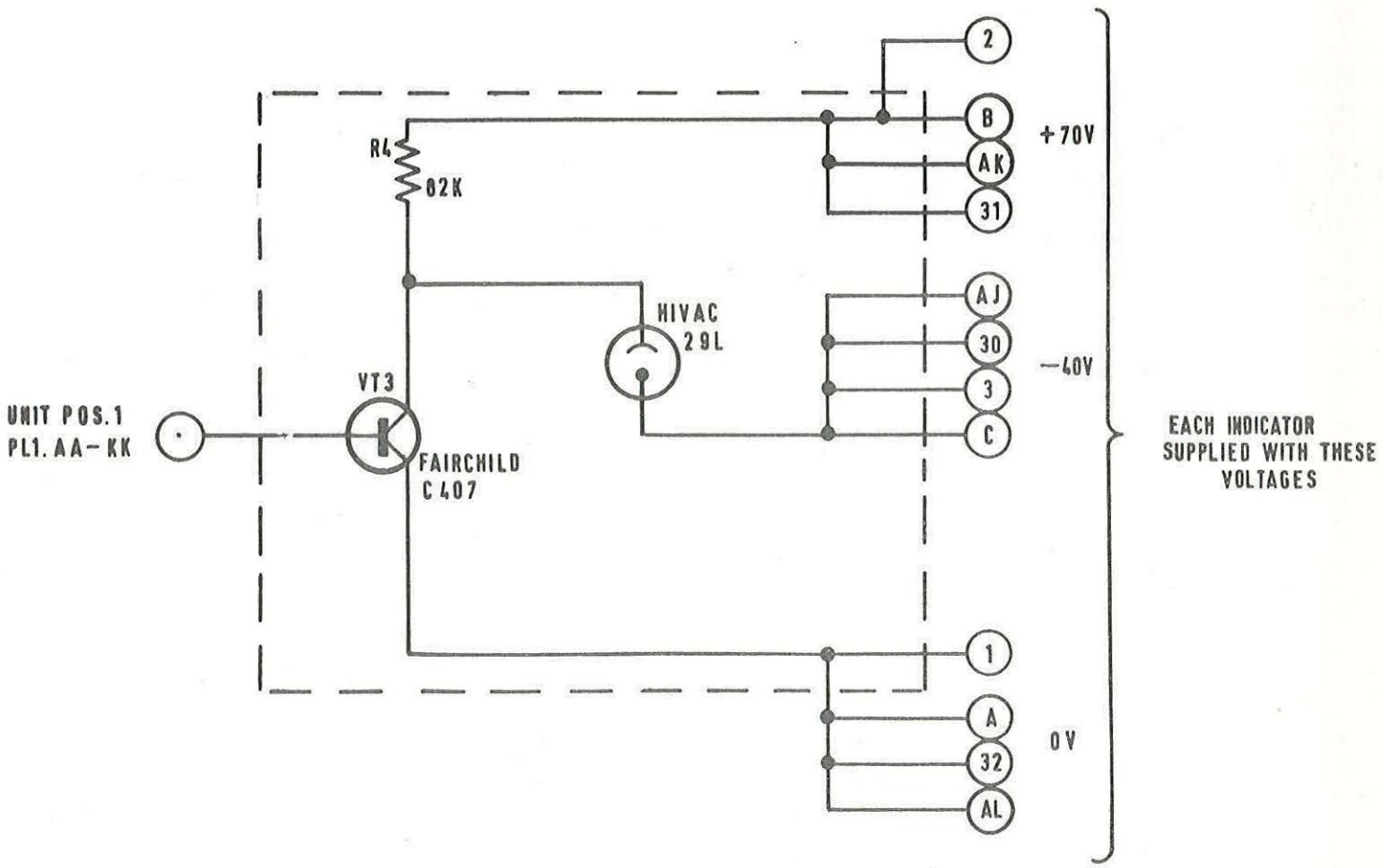
Indicator drive comprises a current limiting resistor R4, a Hivac Neon lamp and VT3, a switching transistor, supplied with +70V, -40V and 0V. The circuit arrangement is depicted in Fig. B.

If VT3 is switched-off, with less than 0.5V on the input, the potential difference across the series connected R4 and the Hivac lamp is 110V, striking the neon. The voltage on the collector will be approximately 40V depending on the burning voltage of the neon.

If VT3 is switched-on with greater than 0.7V on the input, the collector voltage will be less than 5V. The voltage across the neon is then reduced to less than 45V which is insufficient to keep the neon burning.



CONTROL UNIT LAMP DRIVER FIG.a.



INDICATOR DRIVER DISPLAY UNIT FIG.b.

ISS. 1.

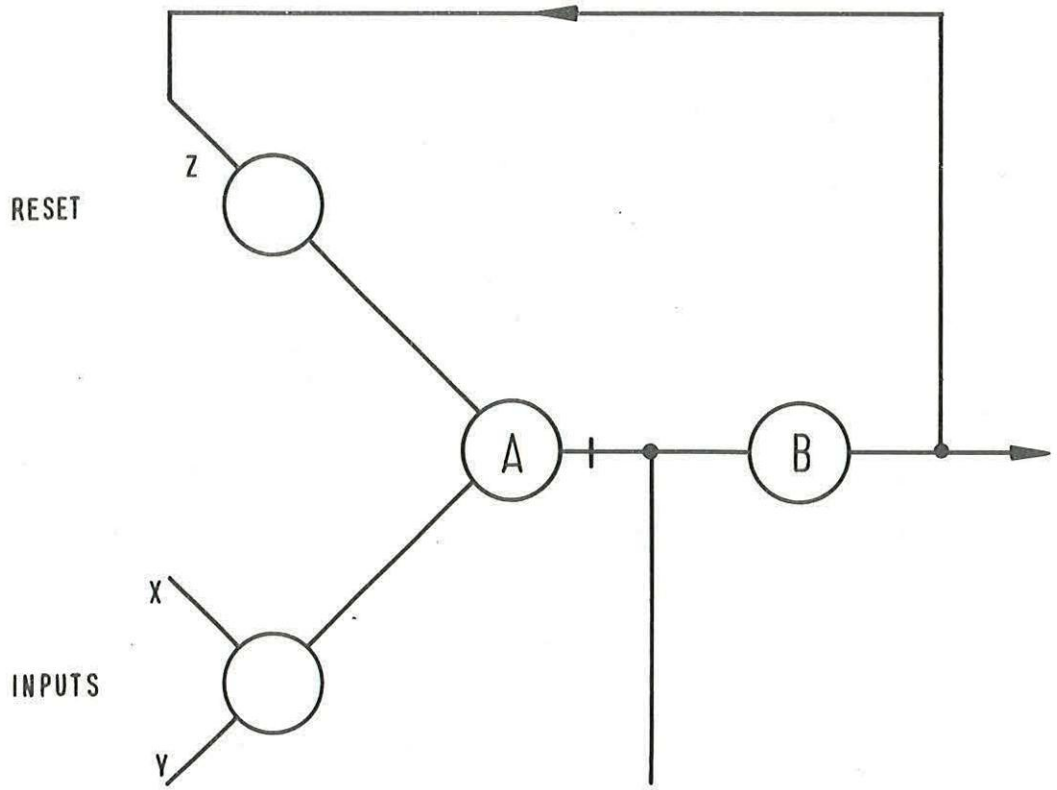


FIG. c. BISTABLE ELEMENT.

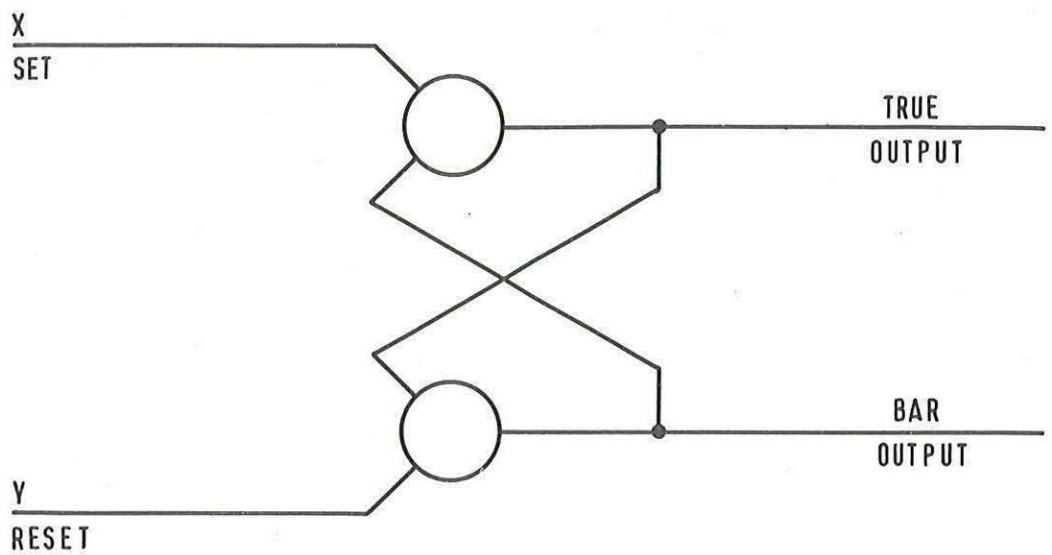


FIG. d. STATISISER.

ISS. 1.

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE No. MCB 143

PART 1: CENTRAL PROCESSOR

CHAPTER 3: THE REGISTER SYSTEM

CHAPTER 3

THE REGISTER SYSTEM

CONTENTS

LIST OF FIGURES

CHAPTER 3

THE REGISTER SYSTEM

1. GENERAL

The Register System of the 920B Computer is an assembly of several basic registers and specialized circuits by which an instruction is implemented in accordance with a specified micro-program to process data. During arithmetic operations information may enter the X and Y inputs of either the adder or collate unit. The X inputs arise from registers M and J and the Y inputs are derived from registers A and Q. The sum of the inputs (X + Y) is fed into the accumulator via buffer register G, from which results are extracted.

The system contains an 18 bit parallel logic adder, with full carry and overflow detection. (The overflow logic is utilized to determine the block of micro-instructions to be followed and enables the detection of conditions for left or right shifting in the operations of multiplication and division). The results obtained set the G-register via direct, left or right shift gates.

Access of information to the Register System is by means of the following:-

(i) Input Channels PTG_1 and PTG_2 convey data from Peripheral devices to the G-Register.

(ii) The M-Register to which information from specified store locations is taken.

Engineer's instructions are set-up in the Register System via a Word Generator in the Control Unit, the output of which is fed into the bistables of the M register.

Instructions comprising an 18 digit word in binary form (pecifying the operation to be performed) are divided nto three groups representing the modifier B = 0/1 the function F = $0 \leqslant F \leqslant$ 5 and the address N $0 \leqslant N \leqslant 8191$.

The address register J is set-up with 13 N digits, the I-register with 4 F digits and t e eighteenth digit for B-modification is i itially held in the M-register.

Input information is incident at the gates of the G-register and output information from the Accumulator direct. A diagram of the structure appears in Fig. A4, which depicts the elements of the Register System connected in the form of a loop, arranged so that information is circulated between appropriate registers during the processing of instructions.

For a complete circulation of data around the loop of registers, six-pulse periods are used with delay periods dependent upon the micro-instructions to be obeyed. The six timing strobes are designated t1 to t6. Strobes t1 and t3 set the reset waveforms, t2 and t4 are "set" strob s and t5 initiates the store cycle. The time delay periods are termed T1, T1 + T2, T1 + tz1 + 470 ns and store cycle delay. T1 is 470 ns, T2 is 300 ns and t3 is 100 ns long.

The control equ.nce for each block of micro-instructions is initiated by the pulse train t6, t1, t2, t3, t4, t terminating with the fall of t5. The incidence of the following t6 pulse initiates a further sequence of micro-instructions. The store cycle is triggered by a t5 strobe. Between the fall of the t6 pulse and the rise of the t1 pulse of the following cycle, the time periods T1, T2 or tZ1 as delay periods may be implemented.

2. CONSTRUCTION

The Register System is an assembly of the following 18 printed circuit logic boards with the elements of the process counter mounted on three additional boards, and the overflow unit on portions of two further boards as tabulated below.

TABLE 1

	THE REGISTER SYSTEM
Unit	Description
A-FA	G-Register (18 bits) 1 bit per board
A-FA	J-Register (16 bits) " " " "
A-FA	M-Register (18 bits) " " " "
A-FA	Q-Register (18 bits) " " " "
A-FA	A-Register (18 bits) " " " "
A-FA	For Adding Unit (18 bits) 1 bit per board
A-FA	P-Register (13 bits)
A-FA	I-Register (4 bits)
A-FP	Process Counter Logic, on three adjacent boards
A-FK	Overflow Unit Portion of board
A-FM	" " " " "

The position of the register boards within the computer is given in Fig. A. 3. The boards are printed circuit types with discrete logic units positioned to an alphabetic plan and colour coded to identify the logic units. Each register board is designed to completely process a single digit of information and therefore carries all pertinent registers. The register logic associated with a single digit of the computer word

and the relationship between such a digit and the register system as a whole is illustrated diagrammatically in Fig. A7 and Fig. A9. Thus in a parallel mode one digit exemplifies the arrangement for the whole.

3. POWER SUPPLIES

The operational power of the Register System is supplied by stabi ized units in the following ratings.

+ 6V d. c. at 7 Amps

- 6V d c. at 3 Amps

A 0V d. c. connection

The standard pin connection on all LSA boards are Pin 21 for +6V, pin 22 for -6V and pin 23 for 0V.

4. THE PRIMARY REGISTERS

4. 1 The G-Register

The G-Register performs a buffer function accepting inputs from the adder, collated adder inputs and external input. Its output is routed to the registers A, Q M and J When strobed it enables the manipulation of operands between registers in computing sequences and receives the output of the Adding Unit, which is the f'nal element of the loop return.

4. 1. 1 The Circuit

The G-register utilizes two LSA 05 and an LSA 01 connected to form a bistable. The direct outputs are routed to the A, Q, M and J-registers and the inverse outputs to the relevant G-register indicators, which may be connected to a display unit. Circuit details are de icted in Figs A7 and A10.

There are six AND gates to each digit position in the G-register. Two input channels, IPn and IP'n are accommodated as are the inputs from the Adding Unit Fn, F(n-1), F(n+1) and the output from the collate unit.

If the incident pulse at input IP (gated by PTG1) is a one, then the output of the G-register (G_n) to the Q, A, M and J -registers will be one. Conversely the incidence of a zero pulse will result in a negative going pulse at the output of the G-register.

The waveforms incident to the G-register and their effects are tabulated in Table 2.

TABLE 2

Waveforms pertaining to the G-register

Reset by waveform OTG which occurs at t1 time				
Set by waveform FTG with F-Unit output at t2 time				
"	"	"	LTG " "	output shifted left at t2 time
"	"	"	RTG " "	output shifted right at t2 time
"	"	"	VTG " "	input (Collate begins)at t2 time
"	"	"	PTG_1	with external input at t2 time
"	"	"	PTG_2	with tape reader input at t2 time

4.2 The M-Register

The M-register functions as an 18 digit stores access register buffering read/write information to the store. Read out operations from the store place information into the M-register. Information read from a specific address in the store must be written back into the same address so that it is not lost. With the M-register set, the write logic circuits are arranged to place 1's into the addressed location in the digit position set by 1's in the M-register.

The facilities available on the Engineer's Control Panel enable verification of the correct functioning of the computer. This check out is accomplished by transmitting the output of the word generator into the M-register (WTM) where it can replace an operand from the stores. This input will enter the W gates.

A subtract facility is also available with this register utilizing the $\overline{M}$ or inverse output in the system "negate and add".

4.2.1 The Circuit

The circuit logic features a triple-input AND/NOR LSA 05 configuration feeding into a single LSA 02. With feedback to the input resulting in a bistable function.

The actuating waveforms appear in Table 3.

TABLE 3

Action waveforms pertinent to the M-register

Reset by waveform	$\overline{\text{OTM}}$ occurring at time t3
Set by waveform	GTM occurring at time t4
Set by waveform	WTM with output from word generator (W_n)
Set by	$\overline{\text{Store n - x}}$
Set by	$\overline{\text{Store n}}$

The logic circuits of the M-register on a single A-FA board is that of a single digit. The logic circuit of the M-register is delineated in Fig. A9.

4.3 The Q-register

The function of the Q-register is that of an auxiliary

register primar'ly used as an extension of the A-register or Accumulator for the temporary storage of information during computation.

When the process of multiplication is implemented, the Q-register holds the least significant part of a product on the occasions where it exceeds the compass of the Accumulator.

If the information in the Q-register is to be preserved, a Function 3 instruction must write this information into a specified address in the core-store.

During the process of division, the dividend is initially placed in the Accumulator. On the occasions where more than 18 digits occur, the least signifi ant bits are placed into the Q-register.

If B-modification is to be performed, the Q-register will hold the N digits of an instruction address that is to be modified.

4.3.1 The Circuit

The logic configuration of the Q-register, one LSA 06 with feed-back to the input resulting in a bistable function. The actuating wavef orms appear in Table 4.

TABLE 4

The actuating waveforms pertinent to the Q-Register.

Reset by $\overline{\text{OTQ}}$ which occurs at t3 time
Set by GTQ which occurs at t4 time
Output gated by QTF as determined by Function

The logic circuits of the Q-register are depicted in the logic drawing Fig. A9.

4.4 The A-register

The A-register or accumulator is the recipient of the results of all arithmetic computations. Interstage or partial products also remain in the accumulator until transferred to the G-register by the gating waveforms ATF and FTG when commencing a subsequent stage of computation.

Facilities available in the 920B Computer determine its operation in one of four program levels (1, 2, 3 and 4) graded in order of priority. If the priority level is higher than the current program, any of the three former program levels may be entered by an INTERRUPT facility.

If, because of exigency a low priority program is interrupted for one of higher priority, measures must be taken to store the contents of the accumulator to preserve its identity. On such occasions, the content of the accumulator is written into a specified store location where it remains until the interrupted program can be continued.

The result obtained at the termination of a computing sequence is taken from the inverse or bar output of the accumulator bistables and routed through cable transmitters to drive the peripheral device.

4.4.1 The Circuit

The logic circuit of the A-register is one LSA 06 with feedback to the input resulting in a bistable function. The actuating waveforms are tabulated in Table 5.

TABLE 5

The actuating waveforms pertinent to the A-register.

Reset by $\overline{\text{OTA}}$ which occurs at t3 time.
Set by GTA with G_n occurs at t4 time.
Output gated by ATF as determined by function.

The logic circuits of the A-register appear on Fig. A9.

4.5 The J-Register

The J-register functions as a 16 bit Store Address Register, and is also used to set the Process Counter.

4.5.1 The Circuit

The logic of the J-register comprises one LSA 06 with an output to the adding unit. Feedback from output to input AND gate forms the bistable element. The action waveforms of the J-register are tabulated in Table 6.

TABLE 6

The Action waveforms pertinent to the J-register.

Reset by $\overline{\text{OTJ}}$ which occurs at t3 time.
Set by GTJ with G_n which occurs at t4 time.
ETJ sets up either SCR or B-register depending on state of K1.
KTJ sets up the J-register to the count of 17 or 18 depending on the state of K2.
JTF transfers contents of J-register into F-unit (adding unit.)

5. THE SECONDARY REGISTERS

5.1 The I-Register

The function of the I-register is to hold the binary digits 14-17 which are the Function digits of the instruction being processed, so that the relevant micro-programmed instruction may be decoded by the control unit. The 4 bit positions in this register are designated I_1 to I_4, with I_1 corresponding to bit 14 of the instruction.

The 16 functions (0-15) are binary coded decimal integers thus:-

Function 0. "Set B-register" appears as $\overline{I_1}$, $\overline{I_2}$, $\overline{I_3}$, $\overline{I_4}$

Function 1. "Add" appears at I_1, $\overline{I_2}$, $\overline{I_3}$, $\overline{I_4}$

Function 2. "Subtract" appears at $\overline{I_1}$, I_2, $\overline{I_3}$, $\overline{I_4}$

⋮

Function 15. "Input and Output" appears at I_1, I_2, I_3, I_4

5.1.1 The Circuit

The logic circuit of the I-register is based on the LSA 06. The feedback formed bistables are utilized in the I-register to generate the necessary decoding waveforms for the selection of the micro-instructions specified.

There are certain areas on the A-FA printed circuit boards that function as either an I or P-register depending on the position in which the board is located.

The circuit comprises one single digit logic to each of the four A-FA boards. Digits I_1, I_2, I_3, I_4 being on A-FA boards 14-17 respectively.

$\overline{\text{OTI}}$ clears the I-register as time t1.

MTI sets the I-register according to digits 14-17 of the M-register at time t2.

5.2 The P-Register

The function of the P or Peripheral Address register is to address the specified peripheral device in Block Transfer and Input/Output functions. The P-register is a unit of 13 digits.

5.2.1 The Circuit

The logic of the P-register is identical with that of the I-register, its function being determined solely by the board position in the computer. The 13 digits appear on A-FA boards 1 to 13.

$\overline{\text{OTP}}$ clears the P-register at time t1.

MTP sets the P-register according to digits 1-13 of the M-register at time t2.

6. SPECIAL PURPOSE REGISTERS

6.1 The Process Counter

The Process Counter is a register of 12 digits which functions as a counter subtracting the number of steps taken during arithmetic processes and shifting operations and also subtracting the number of words occuring during Block Transfer functions.

6.1.1 The Circuit

The logic elements of the Process Counter are mounted on the printed circuit boards 23-25/A-FP. These units comprise four LSA-07 and four LSA-01 in bistable configurations. Input to the Process Counter is via the $\overline{Jn}$ outputs of the J-register.

6.1.2 Multiplication and Division

If waveform K2 is down, the incident waveform KTJ sets-up the J-register to 17. If K2 is up, the J-register is set to 18. When the incident waveform JTPC goes up, the Process Counter is set-up to 17 for multiplication or to 18 for division. The incidence of TPCO at every cycle tests the Process counter for zero, thereby determining the number of cycles to be executed to complete the operation.

6.1.3 Shifts and Block Transfer

If the instruction is a shift, the content of the J-register is used to set the Process Counter to the number of places to be shifted, or words to be transferred.

6.2 The Collate Unit

The collate unit generates the logical sum of the X and Y inputs to the Adding unit and when strobed by VTG, places the result initially in the G-register. This system possesses the advantage of by-passing the Adding unit with its longer operating time (due to carry propagation) when collating. Any transfer strobe incident to registers J, M, A and Q will load the collate unit with the contents of that register.

The decrementing waveform DTF (which effectively adds - 1 when applied to the Adding unit) is used as the collating constant, and is available from the Y inputs of the Adding unit. (Fig. A9 refers). This waveform divides into two groups, DTF_1 and DTF_2; DTF_1 is the collating constant for bits 1 to 13 and DTF_2 is the constant for bits 14 to 18 inclusive. DTF may be applied to the word at the collate gates (or Adding unit) either individually or collectively. Thus DTF_1 or DTF_2 can be used by the micro-program to collate out either the B, F or N component of an instruction.

As an example, to collate out the N component (bits M_1 to 13) of an instruction, bits M1 to 18 are applied to the collate gates via the X input of the Adding Unit. With strobe VTG and collating constant DTF_1 present, a logical AND function is performed on the N b , leaving the address bits unaltered B M_{14} to 18, gated with VTG and $\overline{DTF_2}$ do not sa isfy the AND function thus causing zeros to be set in the B and F positions of the word.

6.3 The Addi g Un t

The Adding Unit receives data from the M and J-reg sters as Xn nputs, the A and Q-registers as the Yn input with outputs of Fn and Cn. Outputs to the overflow unit are from position 37 - C18 and F18, position 56 - F1 and position 38 - C17.

6.3.1 The Adding Unit Inputs

The circuit configuration is such that simultaneous inputs from A or M and J or Q-registers will be automatically added, the result thus obtained sets the G-register in digit positions of relevant significance.

Access to the Adding (F) Unit can only be obtained when gated by specific gating waveforms from the control logic ATF (Accumulator to F), MTF (M-register to F), etc. Input Information, being in the parallel mode is designated An, An+1, An+2, etc. where n is the operand, A the alphabetical pre-fix of the register containing it - A, M, Q or J - and the numerical suffix indicating the Register digit positions from 1 through 18.

The method by which the logic functions of sum and carry are implemented s shown in the logic diagram of a single bit board - Figs. A7 and A9 - in which the term nal numberings are also annotated. The sources of the inputs and outputs are captioned in accordance with the pertinent register and bit numbers. Waveform inputs are titled to

conform with the system of nomenclature used in computers. For example, waveform JTF gates Jn and causes the contents of the J-Register to be transferred to the F-Unit.

In the full or three input adder, the carry-out may be formed from the logical conjunction of any two inputs. The sum may be the result of any one input, from all three inputs, but not from any two inputs.

If a succession of ones is encountered during a carry, the carry must propagate throughout all affected stages. The condition for a succession of carries is that a carry from one stage shall be present together with an input to the next more significant stage.

6.3.2 Operation of the Adding Unit

In order to clarify the operation of the Adding Unit to better advantage, a sequential treatment of signal transfer is herewith given. Emphasis must be placed on the fact that operations are in the parallel mode where similar sequences are carried out concurrently in each of the Adding Unit digit positions.

In Fig. A7 and A9, the Yn input can be generated if any one of the following conditions are satisfied.

(a) A 1 output from digit n position of the Accumulator and Control waveform ATF appear at input AND gate no. (i).

(b) Control waveform DTF appears at input AND gate no. (ii).

(c) A 1 output from digit 1 position of the Q-register and Control waveform QTF appear at input AND gate no. (iii).

A Yn+1 input can be generated in a similar manner.

Similarly a Xn input is generated by the presence of:

(a) A one output from the digit n position of the M-register and Control waveform MTF at input gate (iv).

(b) A one output from $\overline{Mn}$ (Nn) negated digit n from the M-register and Control waveform $\overline{MTF}$ at input gate (v).

(c) A one output from the digit n position of the J-register and Control waveform JTF at input gate (vi).

Inputs n+1, n+2 are derived in a similar manner.

A three input Adding Unit has eight possible input combinations. These are as follows:-

TABLE 7

Input Conditions of the F-Unit.

	Cn-1	Yn	Xn
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

In the following example the operation of the Adding Unit should be read in conjunction Fig. A9.

The logic element C/06-12 is true when $X_n = Y_n$ and false when $X_n = F_n$.

It follows that H/01-13 is only true when Xn=Yn (C/06-12=0) or when Cn-1=0.

Element A/06 is connected so that Fn is only true if the output of C/06-12 and H/01-13 are true (i.e. Xn≠Yn and Cn-1=0) or if the output of H/01-13 and input C_{n-1} is true (i.e. Xn=Yn and C_{n-1}=1).

Then Fn would be true in conditions 2, 3, 5 and 8.

Conditions of Carry:-

The conditions under which Carry occurs is as follows: Cn is true when either the inputs of H/01-1, and H/01-2 are false.

H/01-1 is false when Xn and Yn are true. H/01-2 is false when Xn=Yn and C_{n-1} are true.

It follows from the above statement that the Carry is generated in conditions 4, 6, 7 and 8 of Table 7.

It can be seen from this example that the C_{n-1} digit must be present before the n^{th} stage of addition is correct. During the process of addition, sufficient time is allowed for the Carry to be propogated from bits 1 to 18 of the Adding Unit before transferring to the G-Register.

Instructions may be given, either direct or by micro-program so that digit outputs from the Adding Unit may also be shifted one place left - LTG or right - RTG into the G-register and in this manner the number is effectively doubled (LTG) left shift or halved (RTG) right shift. In cases where a sum greater than 18 digit results, it will go out of range and may be used to set the Overflow Unit. An 18 digit number will also go out of range when a left or right shift is effected, the most significant digit (on a left shift) and the least significant digit (on a right shift) may set the Overflow Unit and be detected by the computer.

6.3.3 The Circuit

The Adding Unit is an assembly of 18 one-digit logic boards of type A-FA arranged in two groups of nine.

The overall logic of the Adding Unit is given by Figs. A7, A9 and A10 and comprises two LSA-06 and one LSA-01.

6.4 The Overflow Unit

The Overflow Unit is a logic extension of the Adding Unit. It is complementary to the Adder and may be set whenever the results of a computation exceeds the limits of the Adding Unit.

The logic diagram of the overflow unit is given in Figs. A8 and A10. The input from Z18, F18 or F1 is selected by the waveforms pertinent to the gate. FTG, LTG or RTG give direct transfer or transfer with left or right shift.

The operation takes place in two stages. In the first, the input sets bistable Y. The second sets bistable X. If required by the micro-program, this data bit can subsequently be transferred to bistable X and later used to set G18 in right shift or G1 in left shift. The actual use will depend upon the instruction which determines the micro-program selected.

6.4.1 The X and Y-Bistables

The operation of the Overflow unit is dependent upon the X and Y bistables. The input to the Y-bistable is at a fan-in of three AND input gates with its output strobed by YTX and cleared by $\overline{\text{OTG}}$. The direct output of the Y-bistable is strobed by YTX in t4 time at the output gate H/02-12. The output of gate H/02-12 is input to the X-bistable which is cleared by $\overline{\text{OTX}}$. The direct output of the X-bistable is gated

by XTF at the gate G/01-2. The output of gate G/01-11 gates K/01-6 giving the output waveform X1. The output of G/01-11 is also inverted by H/03-6 to provide X0.

6.4.2 The Z18 Waveform

The Z18 waveform is the output of two LSA-06 each connected to form an equivalence unit. The output of the first is at J/06-12 as delineated in Figs. A8 and A9. The waveform becomes true when C17 = C18.

The output of the second is Z18 which becomes true when F18 equals the output of J/06-12.

Z18 is true when $F18\ \overline{C17}\ \overline{C18}$ or $F18\ C17\ C18$
$\overline{F18}\ \overline{C17}\ C18$ or $\overline{F18}\ C17\ \overline{C18}$

It can be shown from the above that:

$$Z18 = X18\ \overline{Y18}\ \overline{C17}$$
$$\overline{X18}\ Y18\ \overline{C17}$$
$$X18\ Y18\ C17$$
$$X18\ Y18\ \overline{C17}$$

Z18 is gated with XTF resulting in output X1.

6.4.3 The Shift Function

The output X0 of the Overflow Unit is gated into bit 1 of the G-register by the waveform LTG.

The output X1 of the Overflow Unit is gated into bit 18 of the G-register by the waveform RTG.

In actual operation the shift function is performed upon double-length numbers in registers A and Q, hence the effect of overflow bistable transfer to G will be to carry out the shift operation over from A to Q (right shift) or from Q to A (left shift).

6.4.4 The Circuit

The logic circuits of the Overflow Unit in Figs. A8, A10 comprise two LSA-06 units on the Waveform Driver board 5/A-FR and four LSA-01 units on Store Control and Overflow board 57/A-FM.

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE No. MCB 143

PART 1: CENTRAL PROCESSOR

CHAPTER 4: THE CONTROL SYSTEM

CHAPTER 4

THE CONTROL SYSTEM

CONTENTS

LIST OF FIGURES

THE CONTROL SYSTEM

1. GENERAL

The Control System of the 920B Computer comprises a total of 39 printed circuit boards assembled on racks and arranged as shown in Fig. A3 and Fig. A6. The function of the Control System is to implement a program of computation using the facilities of manual control logic, micro-program, logic program priority control and control of and by peripheral equipment. The circuit of the Control Unit shown in Fig. A22 and the Control System in Fig. A18. The Program Sequence of Functions is laid out in Fig. A11 and Fig. A12.

The computer may be started manually by means of the Control Unit or automatically, by the use of a Start-Address plug. Data may be input either by paper tape or by real-time control channel. The micro-program sequences which are integral with the control system, automatically control the transfers, shifts and store access operations which comprise the complete basic machine code. One of the four priority levels of program working available in the time-sharing system, may be selected by the peripherals when connected to do so. All peripheral equipment is operated under two-way control.

1.1 The Units of the Control System

The board number, nomenclature and functions of the Control Units are detailed in Table 1.

TABLE 1

Logic Boards and their Functions

Board No.	Nomenclature	Function
1	A-FT	Word Generator Input
2	A-FL	Manual Control
3	A-FD	Interrupt
4	A-FC	Pulse Generator and Timing
5	A-FR	Overflow Unit and Timing Drivers
6	A-FI	Conditionals Control Function Drivers
7	A-FH	Matrix Conditionals
8	A-FE	Matrix Amplifiers 1
9	A-FB	Matrix Amplifiers 2
10	A-GJ	Function 15. Control Matrix
11	A-GI	Function 14a. Control Matrix
12	A-GH	Function 14. Control Matrix
13	A-GG	Function 13. Control Matrix
14	A-GF	Function 12. Control Matrix
15	A-GE	Function 7, 8, 9, Control Matrix
16	A-GD	Functions 5 and 6 Control Matrix
17	A-GC	Functions 2, 10 and 11 Control Matrix
18	A-GB	Functions 0, 1, 3 and 4 Control Matrix
19	A-GA	Control Chain
20	A-FG	Matrix Address Drivers
21	A-FF	Matrix Address Logic
22	A-FE	Function Decode and Test P.C.O.
28	A-FO	Cable Receiver 1
29	A-FS	Cable Receiver 2

Board No.	Nomenclature	Function
30	A-FQ	Control I/P, O/P
31	A-FN	Cable Transmitter 1
32	A-FN	Cable Transmitter 2
34	A-FB	Matrix Amplifier
35	A-GL	Initial Instructions 2
36	A-GK	Initial Instructions 1
46	A-FK	W/F Drivers 2
47	A-FJ	W/F Drivers 1
57	A-FM	Overflow Unit and Store Control

1.2 The Power Supplies

The power needed by the Central Processor is +6V d.c. 7A, -6V d.c. 3A and 0V, where all voltages are stabilised.

2. COMPUTER CONTROL CONDITIONS

2.1 Timing

The 920B is an asynchronous type computer, necessitating the pulse and time sequence being predetermined by the programmed instructions.

2.2 Control Logic

The Control Logic Figs. A14, A15, A19 and A21 are overall functional diagrams of the timing unit and the sources of the actuating waveforms controlling the timing unit on the A-FC board. The conditions under which the timer will start are as follows:

(i) When the $\overline{SAO}$ waveform goes false

(ii) When the MST waveform goes false

2.2.1 The $\overline{SAO}$ waveforms

The $\overline{SAO}$ waveform goes false when the following conditions occur.

(i) The Control Unit is connected and the JUMP button is pressed.

(ii) The Control Unit is connected and the ENTER Number Generator key is operated.

(iii) The Control Unit is connected and the OBEY Number Generator key is operated.

(iv) The $\overline{JIA}$ waveform goes false due to either having the switch on the Control Unit set to the AUTO position or having the Start Address Plug connected.

2.2.2 The MST Waveform

The MST waveform goes false when ORDER STOP or CYCLE STOP keys are selected and the RESTART button is pressed.

2.3 Timing Conditionals

The following groups of conditionals may also influence the operation of the timer and are input to Gate A on Fig. A16.

OIS	Order Stop
WFR	Wait for Reply
SB	Store Busy
WFP	Wait for Peripheral
$\overline{Z2}$	Reply Bistable

$\overline{\text{SAO}}$	Set Matrix Address Zero
WTM	Word Generator to M Register
TEST	
SMN	Stop Mode Normal
MST	Manual Step Timer
$\overline{\text{CIS}}$	Cycle Stop Control

2.4 Timer Operation

The timer will operate normally if one input to each gate of timing conditionals remains down. If all inputs to any gate goes up, the output of gate A will go up arresting the timer on the completion of +6. The pulses generated strobe the matrix address logic, function decode logic, waveform drivers, timing drivers, control/function drive, matrix conditionals and interrupt logic in order to maintain the correct time/phase relationship during data processing and computation. Refer to Figs. A16 and A21.

2.5 Timing Conditions

Conditions that hold the timer are depicted in Fig. A15 and described below.

On receipt of the Store Busy signal (SB) (which occurs as a reply to the TR or TW cycle) the gate output remains up until the store cycle has been completed. The timer is therefore held, and any response from the delay chain is prevented from restarting the timer. When the following conditions are satisfied the timer is also held by WFP and Z2 during peripheral transfer and by WFR and OIS when the computer is in the Stop mode or the Order Stop Mode. When CIS (CYCLE STOP) is false, the timer stops at the end of each cycle and is restarted only when MST is false, permitting the input to the first 100 nanosecond pulse generator to be at zero.

2.6 Operation of the Timer

The timer logic is a complex of pulse generators and timing circuits serially arranged and originating positive going pulses of 100 ns width in a six pulse train termed t1' to t6' inclusive. Taps are taken off at the junction of all pulse generators. These pulses are amplified and constitute the strobes t1 to t6. The strobe t6' is routed to another path, where it is amplified, inverted and fed into both a 470 ns delay and a 100 ns pulse delay circuit. The output of this delay is the gating pulse to the peripheral select staticizer on 30/A-FQ unit and also strobes the NAND gate B/01. If a VTG waveform is present at this time corresponding to the 1, or true condition, the VTG timing gate will be open allowing the delayed pulse to originate a zero at the timing reset staticizer. The timer feedback loop responds to a positive going edge when the staticizer is reset. Inversion of this pulse at gate A will retrigger the timing train. However, on the occasions where the VTG waveform does not occur with full adding, an additional 330 ns delay is entered, triggering the timer in response to the changed requirements of these functions.

2.7 920B Timing

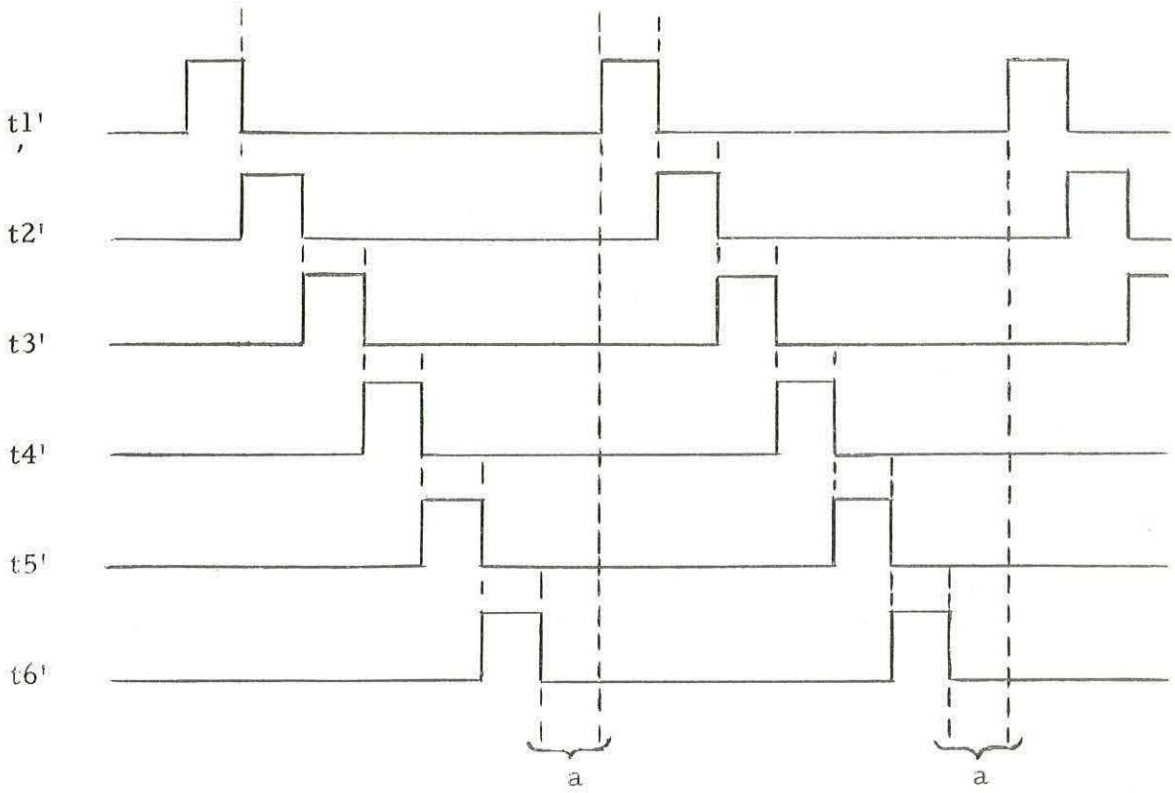


Fig. e Pulses originating at timing generator board 4A-FC.
All pulse widths are nominally 100 ns.

a = 330 ns if VTG
or 800 ns if $\overline{\text{VTG}}$
or until busy is cleared

t1 =	Reset G pulse	46/A-FK W/F Drivers 2
	Reset P pulse	46/A-FK W/F Drivers 2
	Reset I pulse	5/A - FR Timing Waveform Drivers
	Reset pulse to D stat.	(Program (3/A-FD) Interrupt Terminate)
	Reset $\overline{\text{TC}}$ Stat.	(22/A-FE) Function Decode and Test
	Reset AA7 Stat.	(6/A-FI) Conditionals
	Reset CD/CE Stat.	(6/A-FI) Control Function
	(if SFD from Matrix)	Drive

t2	MI pulse	5/A-FR Timing W/F Drivers
	MTP "	47/AFJ W/F Drivers 1
	FTG "	" " " "
	LTG "	" " " "
	RTG "	" " " "
	PTG_1 "	" " " "
	PTG_2 "	" " " "
	VTG "	" " " "
	Set CD/CE Stat. (Test M12/M13 from Matrix)	6/A-FI Conditionals, Control/ Function Drive
	Set T.C. Staticizers and strobe PCO and $\overline{PCO}$ stats.	22/A-FE Function Decode and Test
	Resets E Staticizers	3/A-FD Interrupt
t3	Reset Q pulse	46/A-FK W/F Drivers 2
	Reset A "	46/A-FK W/F Drivers 2
	Reset J pulse	46/A-FK W/F Drivers 2
	Reset M "	46/A-FK W/F Drivers 3
	CO and $\overline{CO}$ pulses	22/A-FE Function Decode and Test
	Set AA1, AA2 and AA3 stats.	21/A-FF Matrix Address Logic
	Set AA7 Staticizer	6/A-FI Cond. Control/Function Drive
	Reset CA' and CB' staticizer	7/A-FH Matrix Conditional Control
	Sets E Staticizers	3/A-FD Interrupt

t4	GTA pulse	46/A-FK	W/F Drivers 2
	GTJ "	"	" " "
	GTM "	"	" " "
	GTQ "	"	" " "
	WTM "	"	" " "
	ETJ "	22/A-FE	Function Decode and Test
	Reset peripheral staticizer	30/A-FQ	Control I/P, O/P
t5	Set CA' and CB' Staticizer	7/A-FH	Matrix Conditionals
	Strobes SFD to set FD	6/A-FI	Control/Function Drive. Conditionals
	Also strobes READ and WRITE Waveforms	57/A-FM	Store Control
t6	Set AA1', AA2' and AA3' Staticizers	21/A-FF	Matrix Address Logic
	Set CA, CB staticizers	7/A-FH	Matrix Conditionals Control

3. THE CONTROL SEQUENCE

3.1 The Micro-program

The Control Sequence on Figs. A11 and A12 is a flow diagram of the micro-program and details the blocks of micro-instructions which control each stage of all computer Functions. Each micro-instruction has a time period from t6 on entering the block until the rise of t6 in the following block. The total time period depends upon the waveforms present in the previous and present block resulting in a variable delay between t6 and t1.

The waveforms for each micro-instruction are produced on the matrix boards by the control or function waveforms, the matrix address, and where necessary the matrix conditionals (see Figs. A16 and A19 SHT. 2).

3.2 The AA1, AA2 and AA3 lines

These lines are outputs from the matrix board in the same manner as the waveforms of the micro-instructions.

They are used to set-up the matrix address of the next micro-instruction to be implemented.

3.3 Matrix Address Waveforms

3.3.1 Normal Addressing

The Matrix address waveforms are SO, S1, S2, S3 and $\overline{S4}$ and in most conditions are derived directly from the AA1, AA2 and AA3 lines.

These lines feed into the matrix address board and are strobed by the t3 strobe to set the intermediate staticizers. If this information is not modified by the action of $\overline{SAO}$, $\overline{CO}$ or AA7, then the output of these staticizers is strobed at t6 time to set the AA1', AA2' and AA3' staticizers.

The outputs of these staticizers enter the 20/A-FG board and are used to originate the matrix address waveforms as in the following table.

TABLE 2

Matrix Address Waveforms

ADDRESS	WAVEFORMS
SO	$\overline{AA2}$, $\overline{AA1}$
S1	$\overline{AA2}$, AA1
S2	AA2, $\overline{AA1}$
S3	AA2, AA1
S4	AA3
$\overline{S4}$	$\overline{AA3}$

3.3.2 Modification by $\overline{SAO}$, $\overline{CO}$ or AA7

(i) $\overline{SAO}$ can only become negative when following the sequence in block C2. On these occasions, it resets the AA2 staticizers thereby setting-up the address for block CO.

(ii) $\overline{CO}$ and CO

These waveforms are both normally up allowing the AA1 intermediate staticizer to be set in the normal way by being strobed at T3. However when a micro-instruction includes the waveform TPCO, this is strobed with the t2 pulse on the 22/A-FE board and used to set the $\overline{TC}$ waveform false. This waveform is then fed into the 21/A-FE board where it inhibits the AA1 line from setting the intermediate staticizers. The P.C.O. waveforms are also strobed by T2 on the A-FE board and are used to set the P.C.O. staticizer.

If the process counter is zero, then during the incidence of the t3 pulse waveform $\overline{CO}$ becomes false setting the AA1 intermediate staticizer true. If the process counter was not zero, then during the t3 pulse time, the CO waveform will become false setting the AA1 intermediate staticizer false. It will be seen from this that the next address can be changed from S3 $\overline{S4}$ to S2 $\overline{S4}$ or from S1 S4 to SO $\overline{S4}$ depending upon the state of the process counter.

(iii) AA7

This waveform is used to change the matrix address from that of the last micro-instruction of any function to the address C2 of Control. The last micro-instruction of each function sets-up the waveforms AA1, AA2, AA3, which would normally set staticizers AA1', AA2', and AA3' in the manner previously described. However the AA1, AA2 and AA3 waveforms are strobed by FD and t3 on the 6/A-FI board and used to set the AA7 staticizer true. The AA7 waveform is then fed to the 22/A-FE board and strobed by t6. This sets the AA1' and AA3' staticizers false setting-up the address of S2 $\overline{S4}$. The AA7 waveform is also strobed by t6 on the 6/A-FI board setting the C/FD staticizers to C.

(iv) TCS (CYCLE REPEAT)

The TCS waveform becomes true when the CYCLE REPEAT key is operated. It prevents the intermediate matrix address staticizers on the 22/A-FE

board from being gated into the AA1', AA2' and AA3' staticizers by the t6 strobing pulse.

The TCS waveform is fed to the 6/A-FI board where it inhibits the setting of the AA7 staticizer. Both the TCS and the $\overline{\text{TCS}}$ waveforms are taken to the 7/A-FH board where the TCS waveform inhibits the resetting of the conditionals by the T3 pulse. The $\overline{\text{TCS}}$ waveform inhibits the $\overline{\text{SFD}}$ waveform so that the C/FD staticizer cannot be set.

From the above it can be seen that Cycle Repeat can be carried out in any block of the Control Sequence.

3.4 The Matrix Conditionals

The Matrix Conditional logic is controlled by both the Manual Controls and the logic of the Control Sequence to implement the desired micro-program.

The selected Conditional Waveforms from CA, $\overline{\text{CA}}$, CC, CB, $\overline{\text{CB}}$ enter the Matrix having been generated by a fan-in of initiating waveforms, which are further discussed in the following sections, see Fig. A16.

3.4.1 Fan-in to Gate A board 7/A-FH

There are six-dual input NAND and two triple input NAND gates performing an OR function fanning-in through an inverter into gate A. All test waveforms arise from the Matrix Amplifiers.

Gate 1 — Gating Number Generator to Accumulator (NGA) with TEST NGA.

Gate 2 — Gates M13 with Test M13. (Block transfer and input-output decode).

Gate 3 Gates $\overline{X}$ bistable with M18 (Division Conditionals)

Gate 4 Gates the output of gate 3 with gate 5 and Test X M18 Division Conditionals.

Gate 5 Gates X bistable with M18. (Division Conditionals).

Gate 6 Gates M18 with Test M18. (B-Modification).

Gate 7 Gates M12 with Test M12. (Shift and input/output).

Gate 8 Gates $\overline{Q}$ with Test XQ_1 and X. (Multiplication)

The output of these gates will enter inverter to Gate A.

3.4.2 Fan-in to Gate B

There is a triple input NAND and a single input NAND gate operating an OR function fanning into an inverter and gate B.

Gate 9 Gates TXQ_1 with $\overline{X}$ and Q1

Gate 10 Gates M_{11} with Test M_{11} (Input/Output).

The output from any of these gates enters an inverter to gate B.

3.4.3 Setting of CA and CB Staticizers

The incidence of t5 pulses together with a conditional waveform sends down gate A output setting the intermediate bistable. The output of this bistable is strobed on the rise of t6 setting the final bistable. The set output of this bistable enters an inverter and is input to a pair of drivers with paralleled CA outputs.

The bistables of gates A and B are set in a similar manner. The inverse outputs of the CA and CB staticizers are gated making CC true when CA and CB are both false.

3.4.4 Reset of Matrix Conditionals

Both intermediate bistables can be reset by the computer reset waveform. These bistables are usually reset by the waveform result of strobing the inverted CRS signal with t3. The final bistables are reset by the waveform result of strobing the inverse output of intermediate bistables with t6.

3.5 Setting of CD. CE Staticizers

The CD and CE conditionals are opposite outputs of the same staticizer. The staticizer is set so that CE is true before the commencement of any function by the waveform SFD gated with t1. The staticizer can be set so that CD is true when M12 = M13 and the waveform TM12M13 is strobed by t2.

3.6 The Function Decode

The Function Decode 22/A-FE is an assembly of eight-triple input NAND gates each feeding into inverting drivers and output into the control matrix. The waveforms generated are DA, DB, DC, DD, DE, DF, DG, DH. These arise from combinations of gating together the series I1, $\overline{I1}$ ——> 14, $\overline{14}$ and with the gates strobed by FD to allow access to the control matrix.

I1	is	gated	with	I2	and	strobed	by	FD	to	originate	Waveform	DA
I1	"	"	"	$\overline{I2}$	"	"	"	"	"	"	"	DB
$\overline{I1}$	"	"	"	I2	"	"	"	"	"	"	"	DC
$\overline{I1}$	"	"	"	$\overline{I2}$	"	"	"	"	"	"	"	DD
I3	"	"	"	I4	"	"	"	"	"	"	"	DE
I3	"	"	"	$\overline{I4}$	"	"	"	"	"	"	"	DF
$\overline{I3}$	"	"	"	I4	"	"	"	"	"	"	"	DG
$\overline{I3}$	"	"	"	$\overline{I4}$	"	"	"	"	"	"	"	DH

4. PROGRAM CONTROL

4.1 Priority Control

The allocation of the Priority Control within the computer is implemented by means of the Interrupt logic (of the Control System) in response to demands from :

(a) the peripheral equipment

or

(b) the Control Unit.

Program 1 is the highest priority and cannot be interrupted

Program 2 can interrupt programs 3 and 4

Program 3 can interrupt program 4 only

Program 4 has the lowest priority and operates when no action is required on levels 1 to 3.

These interrupt demands may either be signalled automatically or manually and cause the next instruction taken by the computer to be obtained from the appropriate level S. C. R.

Lower priority demands are stored during an Interrupt until the corresponding program is re-entered.

Note: The sequence of instructions required for ensuring that the contents of the A and auxiliary registers are stored on the incidence of an Interrupt, and subsequently recovered on its termination are as set out in Table 3.

TABLE 3

Interrupt Conditions

Location	Instruction		Remarks	Sequence
	Function	Address		
[N-6]	-	-	Store for lower level AR	
[N-5]	-	-	Store for lower level ACC	
[N-4]	* 0	N-6	Reset lower level AR	
[N-3]	14	1		
[N-2]	4	N-5	Reset lower level ACC	
[N-1]	15	7168	Terminate. Note SCR. reset to N.	Ter.
INTERRUPT ENTRY, N	5	N-5	Store lower level ACC	Start
[N+1]	3	N-6	Store lower level AR	"
[N+]	-	-	Required program (x locations)	"
[N+2+X]	8	N-4	Jump to reset for level	"

If the contents of the AR on the lower level are not required then instructions N-4, N-3 and N+1 can be omitted and store location N-6 is not required.

It should be noted that bit 1 of the Q-Register is not recovered. This digit is meaningless when it holds part of a double-length product or dividend.

* An interrupt cannot occur immediately after a 0 function because the contents of the auxiliary register has not yet been recovered correctly.

The three program levels on which the interrupt is effective must end with a special instruction (15 7168) which releases the relative priority level and permits the program of the next lower priority to proceed.

The four Sequence Control Registers located at 0, 2, 4 and 6 of the Store, hold the address of the next instructions to be obeyed at each program level. The address of the pertinent SCR originates in the Interrupt Logic. On the occasions where there are no Interrupt demands, the SCR for Program 4 will be automatically selected.

On Fig. A11 the commencement of a program entering either block C0 or C2, will initiate DTE, the test for interrupt. Interrupts will not be implemented until the current instruction has been obeyed, thereby preventing loss of information in the interrupted program.

4.2 Program Level Control

The effect of an interrupt demand on program organization may be seen in the following example, where it is assumed that the contents of the Auxiliary register need not be recovered.

Assume that a program is in operation on level 4, the SCR of which specifies location 25 as the address of the next instruction. The completion of this instruction will increment the SCR by one, making the store location 26, which is the next instruction to be obeyed. The program will continue in this manner until completion, unless an interrupt demand is occasioned.

The occurrence of an Interrupt demand at Program Level 1, causes the Control Logic circuit to set the SCR address to 0 . At the conclusion of this current instruction - 26 in Program Level 4, the computer will read the SCR pertaining to the Interrupt program. Assume that the SCR of Program Level 1 contains 250 as the address of the location holding the next instruction, then the instruction at that address must be Store Accumulator. This preserves the Accumulator Content until Program Level 4 is resumed.

Interrupt Program 1 will now be executed, and on its conclusion, the following instructions are given:

(a) Read Accumulator

Return the stored accumulator content relevant to Program Level 4 to the accumulator.

(b) Jump to 249

Location 249 is the store address holding the terminating instructions 15 - 7168 which is required to release the interrupt, and hence allow the computer to revert to Program Level 4. The SCR now contains 250 having been reset to the address of the first instruction of the interrupt program level.

The resumption of Program Level 4 will place the computer at instruction 27. Program Level 4 will then continue from the point at which it was interrupted.

Fig. A15 and Fig. A18 show the arrangement for the selection of the SCR addresses by the Reset and Interrupt signals.

4.3 The Interrupt Waveforms

The Interrupt waveforms INT1, INT2 and INT3 establishing program priority are output from the Control logic into the PROGRAM INTERRUPT logic unit 3/A-FD. See Fig. A17. These priority waveforms together with $\overline{PS1}$, $\overline{PS2}$ and $\overline{PS3}$ are strobed by $\overline{DTE}$. On the occasions that all these waveforms become true, the pertinent gate will open and the output waveform will set the intermediate bistables. The direct output of these bistables is transferred to the E-bistables when strobed by DTE and t3.

4.3.1 PTR

PTR and t3 are inputs to a NAND gate, the output of which resets a staticizer so that the ensuing test for Interrupt resets the intermediate staticizers at t1 time.

When the function decode waveforms DD and DH are true (or set the B-register function) a staticizer is set, its output inhibits the transfer of the intermediate bistable output to the E staticizers. This staticizer is not reset until DTE is strobed with t4. This means that the next instruction to be obeyed after a set B-register function will be on the same level as the set B-register instruction.

Normally the E-bistable outputs are routed to digit positions 2 and 3 of the J-register to give an address of 0, 2, 4 or 6 dependent upon the state of the E-bistables. READ will then access the content of the store location selected to place this instruction in the M-register.

4.4 The Sequence Control Registers

Both the Sequence Control and B-Registers associated with each program level is tabulated in Table 4.

TABLE 4

SCR, B-Register and Program Levels

Program No.	SCR Address	B-Register Address
1	0	1
2	2	3
3	4	5
4	6	7

On the initiation of a program, an instruction is written into the SCR at that program level to select a point in the program relative to the operations to be performed. The SCR is automatically incremented by one at the commencement of each instruction to be processed. This sequence continues until the program is either completed, or an Interrupt demand occurs.

The Control Sequence, Fig. A11, delineates the method by which the SCR is read and incremented and in Fig. A12, Function 11, the method of storage of the SCR.

4.5 Jump Instruction

The Jump instruction is defined as the direction taken by a program that deviates from the normal program sequence. In this Instruction, the contents of the register is replaced by an address specified by the N-digits of the Jump instruction. Therefore the next instruction to be processed will be the contents of the store location addressed by the N-digits of the jump instruction. Conditions may be specified to define the point at which a jump can occur.

Examples of the jump instruction are given in Chapter 1, para. 7, INSTRUCTIONS, and the Specifications for the 920 Model B computer.

4.6 B-Register

If the instruction contains a number with the digit 1 in the 18th digit position, the B-register will be selected at position C6A. The address of the B-register will be formed by the SCR address of the same level with the addition of KTJ_1. KTJ_1 is generated from the Matrix by the incidence of the K1 and ETJ waveforms placing digit 1 into digit 1 position of the J-register. Therefore the B-register Address for Program Level 1 will be $ETJ_2 = 0$, $ETJ_3 = 0$, plus $KTJ_1 = 1$ and the B-register for Program Level 4 will be $ETJ_2 = 1$, $ETJ_3 = 1$ plus $KTJ_1 = 1$ giving a store address equal to 7. See Fig. A18.

The B-register contains the modifier, and when selected, the contents of this register are added to the N-digits of the instruction selected by the SCR. The F-digits are not affected by B-modification.

5. COMMENCEMENT OF A SEQUENCE OF COMPUTATION

The commencement of a sequence of computation is determined by the input condition of the switches of the Control Unit. In the TEST position all switches on the Control Unit will operate.

For normal operation set the starting address on the NG keys and press the Jump button. In this condition the computer will execute Function 8 placing the address into the SCR.

Under normal conditions, an address obtained from the SCR will be available at the start of the computation cycle. This address then is that of the next instruction to be executed by the computer, and is relative to Level 1. See Fig. A11.

An order can be said to commence either at Block CO or C2 of the Control Sequence - Block C2 is utilized when a program is running and thus constitutes a point at which the next instruction to be obeyed is obtained from the store. Block CO is the point of entry when a starting address or instruction is supplied by the Word Generator of either the Control Unit or the Engineer's Control Panel in place of the store.

The Control Sequence details the following operations:

(a) Extract and Increment of SCR - C2, C3

(b) Extract Instruction C4

(c) Test for B-Modification C5

(d) Extract B-register and modify instruction C6A, C7

(e) B-Modification not necessary C6B

When an instruction is normally concluded, it returns to the quiescent position at C2 of the Sequence pending a further instruction.

5.1 Extract and Increment the SCR

BLOCK C2

This is the first significant point in extracting and incrementing the SCR. The micro-instruction OTM is generated to clear the M-Register of its former content. DTE the Test for Interrupt establishes the priority of the program. ETJ sets the two digit address of the SCR into the J-Register. The Read trigger accesses the location specified and places the contents of the SCR into the M-Register.

BLOCK C3

MTF, ITF, $\overline{\text{OTG}}$, FTG, $\overline{\text{OTM}}$, GTM, WRITE. The micro-instructions originated at this position provide the logic to increment the M-Register.

The contents of M is now written into the SCR by the micro-instruction WRITE. The decoding of the matrix for the next instruction occurs at this point.

5.2 Extraction Instruction

BLOCK C4

MTF, DTF_1, DTF_2, OTG, OTJ, OTM, GTJ, READ, WRITE. Because the incremented SCR in the M-Register pertains to the Next Instruction but One, it is necessary to revert to the now current instruction by decreasing the M-Register control by one. This is accomplished by the addition of -2^{-17} DTF_1, DTF_2. The sum of the former, placed into the G-Register (FTG) is therefore the address appropriate to the instruction to be obeyed. GTJ, READ. The J-Register will now contain the address of the next instruction and the instruction will be placed in the M-Register in response to READ.

5.3 Test for B-Modification

BLOCK C5 TM18

TM18 tests for B-modification. Where the 18th or most significant of the instruction becomes the digit 1 or M18=1, the B-modification will be selected by setting CA true.

5.4 Extract B-Register and Transfer the F-digits into the I-Register

BLOCK C6A

MTF, DTF1, KI, ETJ, OTG, OTI, VTG, MTI, OTM, OTJ, OTQ, GTQ, READ, WRITE. Where B-modification is to be performed, the C6A block is entered, with the M18=1 condition being satisfied. The B-register, held in the Store locations, 1, 3, 5 and 7 contains the modifier,

however this is relative to the four program levels. Where the B-digit occurs, the contents of the B-register of that program level are added to the N-digits before the instruction is obeyed. This operation has no effect on either the F-digits or the stored instruction.

The waveforms OTI and MTI allow the 4 F-digits to set the I-register. Waveforms MTF, DTF, OTG, OTQ and GTQ collate the 13 address digits from the M-register and place them into the Q-register. Waveforms KI and ETJ set the J-register with the address of the present level of the B-register. The READ waveform causes the contents of the B-register to be read into the M-register.

5.5 Completion of B-Modification

BLOCK C7

The waveforms QTF, MTF, OTG, FTG, OTM and GTM cause the contents of the Q and M-registers to be added together and the result placed into the M-register. The waveform SFD enables the function decode line thus formed to complete the Control Sequence.

5.6 The Control Sequence of Functions

The Control Sequence of all Functions that can be implemented in the 920B Computer are shown in the Control Sequence, Figs. A11, A12, A14 and A20. The blocks depict the addresses, operation and timing, giving rise to operational micro-instructions. The timing of some of the waveforms appear in Fig. D.

Two typical blocks and their contents are shown in the following table.

TABLE 5

Typical Control Sequence

A	Matrix Address = SO $\overline{S4}$ DD DE		
	Operation	Waveforms	Timing
	Transfer Address	MTF	*
	from M-Register	$\overline{OTG}$	t1
	into J-Register,	FTG	t2
	then Read contents	$\overline{OTM}$	t3
	of that address	GTJ	t4
	into M-Register	READ	*
		WRITE	*

B	Matrix Address = S1 $\overline{S4}$ DD DE		
	Operation	Waveforms	Timing
	Transfer A-Register	ATF	*
	into Q-Register,	KTJ	*
	then set-up count	TXQ1	*
	of 17 in the	$\overline{OTG}$	t1
	Process Counter.	FTG	t2
	Set the A-Register	$\overline{OTA}$	t3
	and X-Overflow to	$\overline{OTJ}$	t3
	zero. Compare X	$\overline{OTQ}$	t3
	with Q1.	$\overline{OTX}$	t3
		GTQ	t4
		JTPC	t5

The waveforms of the Control Sequence and their relationship to the timing pulses can be seen in Fig. D. The waveshapes shown are diagrammatic and the ideal shapes shown are not attained in practice. A definite time period elapses before the waveform attains its gating value. Commencing with Block A, the Control Sequence takes place in the following manner.

5.6.1 Block A. Matrix Address SO $\overline{S4}$ DD DE

Transfer the address from the M-Register into the J-Register, then Read the contents of that address into the M-Register.

MTF This waveform begins to rise on the incidence of the t6 pulse, but because of the presence of a charging capacitor in the circuit, the curve is exponential and not a ninety degree perpendicular as shown. A delay of 800 nanoseconds (t1 and t2) is introduced between t6 and the start of the next cycle at t1. This delay is made sufficiently long so that the capacitor may have the time to charge to the required operating potential. If VTG is present, the delay is shortened to 470 nanoseconds. The MTF gate begins to open on the incidence of the t6 pulse and closes on the rise of t6 in the following cycle. The transfer of the digital content of the M-Register to the F-Unit must be completed before the fall of t1, as FTG commences on the rise of t2.

$\overline{\text{OTG}}$ This waveform with a period of 100 nanoseconds falls on the incidence of t1, and rises with t2. It clears the G-Register of its contents and sets it for the next operation.

FTG — This is the gating waveform between the F-Unit and the G-Register. The gate opens on the rise of FTG at t2 and falls with t2. The pulse is 100 nanoseconds long.

$\overline{\text{OTM}}$ — Clear the M-Register. This waveform is initiated by the t3 pulse which is also 100 nanoseconds long.

GTJ — This is the gating waveform between the G-Register and the J or Store Address Register placing the address into the J-Register.

READ — This pulse rises with t6 and falls with t5 of the ensuing cycle. Although the READ pulse is up for the entire period, the Read

$\overline{\text{TR}}$ — action is not implemented until the fall of $\overline{\text{TR}}$. The address being set in the J-Register, the read trigger $\overline{\text{TR}}$ accesses the location specified and places the contents of the Store into the M-Register. The $\overline{\text{TR}}$ waveform falls with the rise of t5, and continues for a period of 330 nanoseconds.

SB — Store Busy is initiated by $\overline{\text{TR}}$ and normally continues for a period of six microseconds.

WRITE — The waveform WRITE is initiated with the rise of t6 and falls with the start of t6 of the ensuing cycle.

$\overline{\text{TW}}$ — Trigger write is initiated at the end of the READ cycle. The pulse has a duration of 330 nanoseconds. $\overline{\text{TW}}$ rewrites the information from M into the store. Between $\overline{\text{TR}}$ and $\overline{\text{TW}}$ there is a delay of a little more than three microseconds. The fall of SB triggers the NAND gate K/01-13, and the output being true gates the input bistables of the timing generator, initiating the pulse train t1 - t6. This sequence can be followed in Fig. A15. The address S1 S4 DD is generated and the sequence is continued in Block B.

5.6.2 Block B. Matrix Address S1 $\overline{S4}$ DD DE

Transfer the contents of the A-Register into the Q-Register then set-up a count of 17 in the Process Counter. Set the A-Register and X-Overflow to zero. Compare X with Q1.

ATF — The ATF waveform rises on the incidence of t6, and falls with the rise of the following t6. This is the gating waveform between the A-Register and the Adding Unit. The transfer of information from the A-Register to the Adding Unit must occur before the rise of t2 when FTG comes true.

KTJ — This waveform sets-up the J-Register. KTJ rises with t6 and remains up until the rise of the following t6. When JTPC goes up the Process Counter is set-up for the count of 17 when K2 is not present, and the count of 18 when K2 is present.

TXQ1 — This is a testing waveform that is utilized in comparing the relationship between X and Q1. This waveform rises with t6 and remains up until the rise of the following t6.

$\overline{OTG}$ — This waveform clears the G-Register and sets it for the next operation. This waveform with a period of 100 nanoseconds falls on the incidence of t1, rising to terminate at the rise of t2.

FTG — The gating waveform between the F-unit and the G-Register. The digits are transferred from the F-unit to the G-Register. The gate opens on the rise of FTG at t2 and falls with t2.

$\overline{OTA}$ — The clearing waveform of the Accumulator. This pulse falls on the rise of t3 and rises with the fall of t3.

$\overline{\text{OTJ}}$ The clearing waveform of the J-Register. This pulse falls on the rise of t3 and rises with the fall of t3.

$\overline{\text{OTQ}}$ The clearing waveform of the Q or Auxiliary Register. This pulse falls on the rise of t3 and rises with the fall of t3.

$\overline{\text{OTX}}$ The clearing waveform of the X-bistable of the Overflow unit setting it to zero. This pulse falls on the rise of t3 and rises with the fall of t3.

CTQ The gating waveform between the G-Register and the Q-Register, transferring the digital content of the G-Register into the Q-Register. This waveform is initiated by the t4 pulses and rises and falls in t4 time.

JTPC This waveform transfers the contents of the J-Register into the Process Counter. The pulse is implemented by the rise of t5, with which it also falls.

6. CONTROL WAVEFORMS

The following waveforms strobe the gating circuits within the computer thereby controlling the process of completion. Their functions are detailed in TABLE 6.

TABLE 6

Control Waveforms

WAVEFORM	FUNCTION
AA1, AA1', $\overline{AA1'}$	Binary count of matrix addresses.
AA2, AA2', $\overline{AA2'}$	Binary count of matrix addresses.
AA3, AA3', $\overline{AA3'}$	Binary count of matrix addresses.
AA7	The result of gating AA1, AA2 and AA3 with timing pulses t3 and FD.
ATF	Gating pulse transferring the Accumulator content into the F or Adding Unit.
CA1, $\overline{CA1}$	Conditional waveforms originating in the Matrix Conditional and D.E. conditionals logic when strobed by the pertinent waveforms.
CA2, $\overline{CA2}$	
CB	
$\overline{CB}$	
CC	
CD	
CE	
CLEAR	Clear the former content of the Store location specified.
CRS	Inhibits the resetting of the conditionals CA and CB by t3.

WAVEFORM	FUNCTION
DTE	Test for Interrupt. Occurs only at the commencement of micro-instructions CO and C2. This allows the Interrupt content of the H and J bistables to pass into the E-bistables thereby forming the SCR address of the interrupt program level.
DTF_1	Places a one input into the Adding Unit in bits 1-13.
DTF_2	Places a one input into the Adding Unit in bits 14-18. 167
Cn	n = 1-18. Carry.
CØ	Counter zero
CON	Continue
CIN	Continuous Number Generator
CS. CIS	Cycle Stop
DA DB DC DD DE DF DG DH	These are waveforms arising from the Function Decode Unit in response to gating waveforms from the I-Register selecting an element in the Control Matrix.

WAVEFORM	FUNCTION
ETJ	This waveform sets the two digit address of the appropriate SCR. The Interrupt contents of the E-bistables are transferred to the J-Register. Sets up SCR from E1 and E2 if K1 is down or false, but sets up B-Register if K1 is up or true.
ENG.	Enter number generator
E1, $\overline{E1}$, E2, $\overline{E2}$	Interrupt addressing
FD	Function Decode
FTG	Strobes the contents of the Adding Unit into the G-Register.
GTA	Gating waveform from the G to A-Register
GTJ	Gating waveform from the G to J-Register
GTQ	Gating waveform from the G to the Q-Register
GTM	Gating waveform from the G to the M-Registers.
INT. LEV. 1k " " 2k " " 3k	Interrupts from Control Unit
INT 1 " 2 " 3	Interrupts from peripherals

WAVEFORM	FUNCTION
IRX IRY IWX IWY	Store drive select read and write currents
IIG	Initial Instruction Gate
IIS	Initial Instruction Strobe
IP	Inhibit Pulse
Jn	n = 1-18. Output of J-Register with J_1', J_2' etc., output from drivers.
JTF	Gating waveforms between J and F-Registers
JTPC	Enter J-Register into Process Counter
JUMP	Instruction utilized to initiate computer cycle placing program trigger in SCR. Refer to ETJ
K1	Sets up J-Register to 17 if K2 is down or false, or 18 is K2 is up or true. Then when JTPC goes up or becomes true, Process Counter is set-up to 17 for Multiply or 18 for divide.
LTG	Gates the Adding Unit content into the G-Register, shifting this content one place to the left doubling the sum.
Mn	n = 1-18. The output of the M-Register.
MTF	Gates the contents of the M-Register into the Adding Unit.

WAVEFORM	FUNCTION
MTI	The extraction of the Function digits M14, M15, M16 and M17. Set the four-digit I-Register to select the specified function.
MTP	Gating waveform between M and 13 digit P-Register
MST	Manual Step Timer
NG	Waveform originated by Number Generator switches NG-1 NG-18 to select Word Generator input.
NGA	Waveform originated depending upon position of Enter Number Generator Switch. The word generator sets the Accumulator.
OA_n	n = 1-18. Output of A-Register to a peripheral
ONG	Obey number generator.
$\overline{OS}$	Order stop
$\overline{OTA}$	Clear A-Register
$\overline{OTG}$	Clear G-Register
$\overline{OTJ}$	Clear J-Register
$\overline{OTM}$	Clear M-Register
$\overline{OTQ}$	Clear Q-Register
$\overline{OTP}$	Clear P-Register
$\overline{OTI}$	Clear I-Register
$\overline{OTX}$	Clear X-bistable

WAVEFORM	FUNCTION
Pn	n = 1-18. Output of P-Register
PI	Peripheral Interrupts
PTG_1	Control Waveform to G-Register gates in IPn from peripheral
PTG_2	Control Waveform to G-Register gates in IP'n from tape reader.
PTR	Program Terminate
PSC	Power Supplies correct
PC_n	Process Counter display n = 1-12
$\overline{PSI}$	Peripheral Interrupt Suppress
$\overline{PS2}$	Generated when the Interrupt Level switches
$\overline{PS3}$	are in Manual on the Control Unit.
Qn	n = 1-18 output of Q-Register
QTF	Gating waveform of auxiliary Q-Register contents into the F-Unit.
READ	The READ trigger accesses the location specified and places the contents into M.
RESET	This waveform returns the computer logic to its initial state.
RESTART	Restart the timer.
RGS	Read Gate Strobe

WAVEFORM	FUNCTION
RTG	Strobes the contents of the F-unit into G-Register shifting this content one place to the right thus halving it.
RTR	Reply from Tape Reader
RTP	Reply from Tape Punch
$\overline{RX}$	Read Strobe to X-Master Driver
$\overline{RY}$	Read Strobe to Y-Master Driver
SO S1 S2 S3 S4 $\overline{S4}$	Matrix Addressing waveforms arising from the Matrix Address Drivers 20/A-FG gated by combination of AA1', AA2' and AA3' and their bar forms.
SB	Store busy
SZ_1	Set peripheral select staticizer
SAO	Set matrix address to zero
STC	Store Temperature Correct
SHO	Store Heaters On
SFD	Set Function Decode Strobing conditionals and Control/Function Drive.
SMN	Stop Mode Normal
$\overline{SSI}$	Store Strobe Inhibit

WAVEFORM	FUNCTION
STR	Select to Reader
STP	Select to tape punch
SIP	Select peripheral input
SOP	Select peripheral output
SIS	Suppress Internal store
STROBE	Sense Amplifier Strobe
t1, t2, t3, t4, t5, t6	Timing strobes output of the timing generator board 4/A-FC. These strobes maintain the correct time and phase relationship during data processing and computation.
TM_{11}, TM_{12}, TM_{13}, TM_{18}, $TM_{12}M_{13}$, TNGA, TXM_{18}, TXQ_1	These waveforms are used to set the conditionals, together with other waveforms they are incident to the gates of the Matrix conditional board 7/A-FH, and are the output of matrix amplifiers 8/A-FB and 9/A-FB.
TPCO	Test Process Count Zero
$\overline{TR}$	Trigger Read to Store
$\overline{TW}$	Trigger Write to Store
TCS	Transfer control stop from Cycle Repeat key on Control Unit.

WAVEFORM	FUNCTION
TC	Test Count
VTG	Transfer the contents of the Collate Unit into G-Register.
$\overline{W}$	Write strobe to X and Y - Master Driver
WFP	Wait for peripheral
WFR	Wait for Restart
WTM	Input word generator to M-Register
WRITE	Write or copy the contents of the M-Register into the store location as specified by the J-Register.
WGS	Write Gate Strobe
X	X bistable of overflow unit
XTF	Gating waveform between the X-bistable and adder or gates a digit in Overflow Unit into the Adding Unit.
Y	Y-bistable of overflow unit
YTX	Gates Y into X-bistable, or if an overflow digit occurs, it is gated into the X-bistable.
Z2	Reply from peripheral
Z18	In Overflow Unit triggering Y and X bistables
ITF	The control waveform originated by matrix to rout the digit 1 to the least significant digit position of the Adding Unit. This facility is used basically in subtraction (Function 2 Negate and Add) in which the negated contents of the Accumulator are added to the contents of the store location as specified by N. The contents of N are also placed in the Q-Register.
1TPC	Subtract 1 from Process Counter.

7. DESCRIPTION OF INDIVIDUAL FUNCTIONS

The brief description of the individual functions given in the following paragraphs serve to demonstrate the method by which the computer performs its operations. The starting point of all operations is the Block C2 commencing with Test for Interrupt (DTE). The computing sequence from blocks C2 to C7 has already been described in some detail. Table 7 gives the Functions and their binary equivalents in the I-Register. See Fig. A11 and Fig. A12.

TABLE 7

FUNCTIONAL TRUTH TABLE

FUNCTION		BINARY EQUIVALENT	FUNCTION DECODE
FØ	Set B-Register	0 0 0 0	$\overline{I1}$ $\overline{I2}$ $\overline{I3}$ $\overline{I4}$
F1	Add	0 0 0 1	I1 $\overline{I2}$ $\overline{I3}$ $\overline{I4}$
F2	Negate and Add	0 0 1 0	$\overline{I1}$ I2 $\overline{I3}$ $\overline{I4}$
F3	Store Q Register	0 0 1 1	I1 I2 $\overline{I3}$ $\overline{I4}$
F4	Read	0 1 0 0	$\overline{I1}$ $\overline{I2}$ I3 $\overline{I4}$
F5	Write	0 1 0 1	I1 $\overline{I2}$ I3 $\overline{I4}$
F6	Collate	0 1 1 0	$\overline{I1}$ I2 I3 $\overline{I4}$
F7	Jump if A=0	0 1 1 1	I1 I2 I3 $\overline{I4}$
F8	Jump	1 0 0 0	$\overline{I1}$ $\overline{I2}$ $\overline{I3}$ I4
F9	Jump if A is negative	1 0 0 1	I1 $\overline{I2}$ $\overline{I3}$ I4
F10	Count in store	1 0 1 0	$\overline{I1}$ I2 $\overline{I3}$ I4
F11	Store SCR	1 0 1 1	I1 I2 $\overline{I3}$ I4
F12	Multiply	1 1 0 0	$\overline{I1}$ $\overline{I2}$ I3 I4
F13	Divide	1 1 0 1	I1 $\overline{I2}$ I3 I4
F14	Shift/Block Transfer	1 1 1 0	$\overline{I1}$ I2 I3 I4
F15	Input and Output/ Program Terminals	1 1 1 1	I1 I2 I3 I4

8. FUNCTION Ø SET B-REGISTER

The function decode is 0000 $\overline{I1}$ $\overline{I2}$ $\overline{I3}$ $\overline{I4}$ to give the instruction: Place the number from the specified store location into the B-Register.

The instruction starts from the quiescent point at C2, the number to be placed in the B-Register is accessed from Store. To preserve this information in the store after a READ operation, a WRITE into the M-Register is arranged. The number is thus replaced in the location while the address remains set in the J-Register.

The logic of the operation may be followed in Fig. A11, Fig. A15, Fig. A16 and Fig. A18.

The operation commences at the quiescent point C2.

C2 DTE - Test for Interrupt. Set the address of the SCR for the level selected by Interrupt. Read the SCR into the M-Register.

C3 Increase the M-Register by 1, and re-write into the SCR.

C4 Decrease the M-Register by 1, then transfer into the J-Register. Read the contents of that address into the M-Register.

C5 In the TM-18 test, M18 is decoded to determine if a B-modification is to be carried out. The J-Register is then set to zero.

C6B Transfer function from M-Register into I-Register and enable a Function Decode to take place.

8.1 Block 00

Transfer the address from the M-Register into the J-Register, then read the number from that address into the M-Register.

MTF, PTF_1, PTF_2, OTG and VTG produces the following. The G-Register is cleared of its contents. The contents of the M-Register are transferred to the Adder, collated into the G-Register, then transferred into the J-Register. OTM clears the M-Register and the READ operation copies the contents of the store location specified by the address N into the M-Register. The WRITE operation copies the contents of the M-Register into the store location specified by the address N. The matrix address generated transfers the operation to the block 01.

8.2 Block 01

Set the J-Register with the address of the B-Register at the existing level. Transfer the number from the M-Register into the Q-Register, and with the M-Register set, the information is written into the B-Register.

The waveform MTF gates the contents of the M-Register into the Adding Unit. $\overline{\text{OTG}}$ FTG clear the G-Register and transfer the contents of the Adding Unit into the G-Register. GTQ transfers the contents of the G-Register into the Q-Register. ETJ, K1 set up the J-Register to the address of the B-Register. CLEAR. The B-Register is cleared of old information. WRITE. This operation writes the contents of the M-register into the B-register. The matrix address set-up by these operations returns the computing sequence to the quiescent point at C2.

9. FUNCTION 1. ADD

The function decode in binary is 0001, with I1, $\overline{I2}$, $\overline{I3}$, $\overline{I4}$ to give the instruction.

Add the number in the specified store location into the Accumulator.

The control sequence is implemented commencing with DTE at C2, continuing through to C6, and if B-modification is necessary C7 is included. The logic of the operation may be followed in Fig. A11, Fig. A16 and Fig. A18.

9.1 Block 10

Transfer the address from the M-Register into the J-Register, then read the number from that address into the M-Register.

The M-Register holds the address of the required operand. One operand is already in the Accumulator. The waveform MTF gates the information in the M-Register into the Adder: DTF_1, DTF_2, OTG, VTG, GTJ give rise to the following. The G-Register is cleared of its existing contents, the address is collated out and placed into the G-Register, from where it is gated into the J-Register. The READ operation extracts the addend or second operand from the store location addressed and places it into the M-Register. The WRITE operation copies the contents of the M-Register into the store location specified by the address N. The Matrix address generated transfers the sequence to Block 11. The logic of the operation may be followed in Fig. A11, Fig. A16 and Fig. A18.

9.2 Block 11

Add the contents of the A-Register and the M-Register, then place the result into the A-Register.

OTG clears the G-Register of its existing contents. MTF, ATF, the addend or second operand in the M-Register and the augend

or first operand in the Accumulator are both routed into the Adding Unit. The resulting sum is transferred to the G-Register by the incident waveform FTG. OTA clears the accumulator, following which the strobe GTA transfers the contents of the G-Register into the Accumulator. The control sequence now returns to the quiescent point at C2.

10. FUNCTION 2. NEGATE AND ADD

This function decode in binary will contain 0010, $\overline{I1}$, I2, $\overline{I3}$, $\overline{I4}$ to give the instruction: Negate and add the number in the store location specified to the contents of the Accumulator.

The control sequence is implemented by commencing with DTE, Test for Interrupt at C2, through to C6 or C7 if B-Modification is required. The logic of the operation may be followed in Fig. A11, Fig. A15 and Fig. A16.

10.1 Block 20

Transfer the address from the M-Register into the J-Register then read the number from that address into the M-Register.

MTF. This waveform strobes the information from the M-Register into the Adding Unit. DTF_1, DTF_2, OTG, VTG, GTJ give rise to the following: The G-Register is cleared of its digital content, and the address is collated out and placed in the G-Register, from where it is gated into the J-Register. The store location containing the minuend is READ and the information being obtained, the minuend is written back into the store specified by the address N. The matrix address generated, then transfers the sequence to Block 21.

10.2 Block 21

Transfer the contents of the M-Register into the Q-Register.
MTF, OTG, FTG. These microinstructions clear the G-Register, then

transfers the digital content which is the minuend from the M-Register to the Adding Unit then from the Adding Unit to the G-Register. The waveform OTQ clears the Q-Register and the strobe GTQ sets the Q-Register with the minuend. The matrix address generated transfers the operation to Block 22.

10.3 Block 22

Transfer the contents of the A-Register into the M-Register.

ATF, OTG, FTG. The waveform OTG clears the G-Register of its existing content and the strobes ATF and FTG transfer the subtrahend from the Accumulator into the G-Register. The strobe OTM now clears the M-Register which so far has held the minuend in addition to the Auxiliary Register. The micro-instruction GTM now places the subtrahend into the M-Register and the operation enters the final stage in Block 23.

10.4 Block 23

Add 2's complement of the M-Register to the Q-Register and place the result into the A-Register. QTF, $\overline{\text{MTF}}$, 1TF, OTG, FTG. The micro-instructions clear the G-Register, and add the minuend to the negated subtrahend also placing the result into the G-Register. Negation is effected by utilizing $\overline{\text{MTF}}$ and the output from the inverse output of the M-Register bistable. The strobe 1TF adds +1 to the least significant digit position to correct the number with respect to the modulus 2. The strobe OTA clears the Accumulator so that GTA may transfer the contents of the G-Register to the Accumulator. The operation is now terminated and returns to the quiescent point at C2.

10.5 A demonstration of the subtraction process is given in the following examples.

10.5.1 Example; Subtract + 1/2 from + 3/8

The Accumulator will contain the subtrahend + 1/2 or 0.1000, the M-Register the minuend + 3/8 or 0.0110.

Block in Sequence	Micro-Instruction	Register	Content
21	MTF	M	0.0110
"	FTG	G	0.0110
"	GTQ	Q	0.0110
22	ATF	A	0.1000
"	FTG	G	0.1000
"	OTM	M	0.0000
"	GTM	M	0.1000
23	QTF		0.0110
"	$\overline{\text{MTF}}$		1.0111
"	1.TF		1
	FTG		1.1110
			= -1/8

10.5.2 Conversely, subtracting +3/8 from the +1/2 will give an M-Register content of 0.1000 and an Accumulator of 0.0110.

Block in Sequence	Micro-Instruction	Register	Content
21	MTF	M	0.1000
"	FTG	G	0.1000
"	GTQ	Q	0.1000
22	ATF	A	0.0110
"	FTG	G	0.0110
"	OTM	M	0.0000
"	GTM	M	0.0110

Block in Sequence	Micro-Instruction	Register	Content
23	QTF		0.1000
"	$\overline{\text{MTF}}$		1.1001
"	1TF		1
	FTQ		0.0010
			= -1/8

NOTE: There can be no digit of greater significance than the sign digit. Where such a digit results from a carry action, it will be out of range.

If an answer goes out of range ($-1 \leq F < +1$) an incorrect result will be obtained.

11. FUNCTION 3. STORE Q REGISTER

The I-Register will contain the binary equivalent of the digit 3 which is 0011 or I1 I2 $\overline{\text{I3}}$ $\overline{\text{I4}}$ to give the instructions. Place the number in the Auxiliary Register in the 17 least significant digit positions of the store location specified and the most significant digit position is made zero.

This function is most frequently used after a multiplication operation where it is instrumental in accessing the Q or Auxiliary register. The programmer cannot address the Auxiliary Register directly. Therefore after a process of multiplication, where a product including the sign digit occupies 35 digit positions of the Accumulator and auxiliary registers, to obtain the 17 least significant digits of the product, a Function 3 must be given. This places the information into a specified store location from which it may be read.

The sign of a product is given by digit positions 18 of the Accumulator. Manipulation of the multiplicand and partial product during

the multiplication sequence results in the Auxiliary register containing the 17 least significant digits of the product in bit positions 2 to 18. Bit position 1 of the Q-Register being of no significance. By means of Function 3 the least significant digits of the product are placed into the store location in a manner ensuring that the sign position is zero. A right shift therefore does not halve the Auxiliary register content in this application.

To implement Function 3, the Control Sequence commences at the quiescent point C2 then through to C6 or C7 where the matrix address selects Block 30. The logic of the operation may be followed in Figs. A11, A15 and A16.

11.1 Block 30

Transfer the address from the M-Register into the J-Register and set overflow unit to zero.

$\overline{\text{OTG}}$ clears the G-Register and MTF, DTF1, DTF2 and VTG collate the contents of the M-Register into the G-Register.

The strobe $\overline{\text{OTX}}$ resets the X-bistable of the Overflow Unit and the waveform GTJ strobes the digital content of the G-Register into the J-Register. The operation is transferred to Block 31 by the generation of the matrix address S1 $\overline{\text{S4}}$ DA DH.

11.2 Block 31

Right shift of the Q-Register by one bit while transferring it to the M-Register. Write the contents of the M-Register into the above address.

$\overline{\text{OTG}}$, RTG, QTF, XTF. The G-Register is cleared of its contents. The Auxiliary Register is shifted one place to the right and placed into the G-Register. The waveforms XTF and RTG transfer the

contents of the X-bistable into the G-register. This makes the sign digit position a zero.

$\overline{\text{OTM}}$, GTM. The M-Register is reset by $\overline{\text{OTM}}$, this clears the M-Register of its digital content. GTM places the contents of the G-Register into the M-Register. The store location specified is cleared by CLEAR. The WRITE operation writes the new M-Register content into the store. This operation completes the Function 3, and returns to the quiescent point at C2.

12. FUNCTION 4. READ

The I-Register will contain the binary equivalent of the digit 4, which is 0100 or $\overline{I1}$ $\overline{I2}$ I3 $\overline{I4}$, to give the instruction: Place the number in the specified store location into the accumulator.

The instruction starts from the quiescent point at C2 through C6 or C7 where the matrix selects Block 40. The drawings illustrating the operation are identical with Function 1.

12.1 Block 40

Transfer the address from the M-Register into the J-Register, then read the number from that address into the M-Register.

MTF. This waveform transfers the contents of the M-Register into the F-Register. DTF1, DTF2, $\overline{\text{OTG}}$, VTG, GTJ. The G-Register is reset and the address is collated out, placed in the G-Register and gated into the J-Register. The store location containing the information is READ into the M-Register and the information thus obtained is Written back into the store specified by the address N. The operation then transfers to Block 41.

12.2 Block 41

Transfer the contents of the M-Register into the A-Register

MTF. The contents of the M-Register are transferred to the Adding Unit. $\overline{\text{OTG}}$, the G-Register is reset by this strobe and the digital content of the Adding Unit is transferred to the G-Register by waveform FTG. The accumulator is cleared by $\overline{\text{OTA}}$, and the contents of the G-Register transferred to the Accumulator by GTA. The operation being completed for Function 4 the sequence returns to the quiescent point at C2.

13. FUNCTION 5. WRITE

The I-Register will contain the binary equivalent of the digit 5, which is 0101 or I1 $\overline{\text{I2}}$ I3 $\overline{\text{I4}}$ to give the instruction:- Place the number in the Accumulator into the store location specified.

To implement Function 5, the Control Sequence commences at the quiescent point C2 through C6 or C7 where the matrix address selects S0 S4 DB DF. Block 50. The logic of the operation may be followed in Figs. A11, A15 and A7.

13.1 Block 50

Transfer the address from the M-Register into the J-Register and set the M-Register to zero.

The MTF waveforms strobe the information from the M-Register into the Adding Unit. DTF1, DTF2, $\overline{\text{OTG}}$, VTG, GTJ. The G-Register is cleared of its digital content and the address is collated out and placed into the G-Register, from where it is gated into the J-Register. $\overline{\text{OTM}}$ clears the M-Register. The operation transfers to Block 51.

13.2 Block 51

Transfer the contents of the A-Register into the M-Register and write the contents into the above address.

$\overline{\text{OTG}}$, ATF, FTG. The G-Register is cleared by the waveform $\overline{\text{OTG}}$ and the digital content of the Accumulator transferred to the G-Register by the waveform ATF, FTG. GTM places the function to be stored into the M-Register. The store location specified is cleared by CLEAR. WRITE writes the word into the store.

This operation concludes the WRITE function, and the Control Sequence returns to the quiescent position at C2.

14. FUNCTION 6. COLLATE

The I-Register will contain the binary equivalent of the digit 6 which is 0110 or $\overline{\text{I1}}$ I2 I3 $\overline{\text{I4}}$ to give the instruction: Place into the accumulator the logical product of the contents of the store location specified and the former contents of the Accumulator i.e. place ones in the Accumulator in only those digit positions in which both the store location contents and the Accumulator contents are ones.

The Control Sequence is implemented by commencing with DTE at C2, continuing through to C6 or C7 if B-modification is necessary. The operation continues in Block 60. The operation may be followed on the same drawings used in Function 5.

14.1 Block 60

Transfer the address from the M-Register into the J-Register then read the number from that address into the M-Register. The series of waveforms MTF, DTF1, DTF2, $\overline{\text{OTG}}$, VTG, GTJ gate the contents of the M-Register into the J-Register. M is cleared and the store location

containing the information is READ and the resultant information Written back into the store. The matrix address is generated and the operation transfers to Block 61.

14.2 Block 61

Transfer the contents of the Accumulator and the M-Register to the collate unit, then place the output of the collate unit into the Accumulator.

Waveforms MTF, ATF transfer the contents of both the M-Register and the A-Register into the Adding and Collate Units.

$\overline{\text{OTG}}$ clears the G-Register, VTG places the output of the collate unit into the G-Register. $\overline{\text{OTA}}$, GTA clears the A-Register and transfers the contents of the G-Register into the A-Register. This operation concludes the collate function and the control sequence returns to C2.

15. FUNCTION 7. JUMP IF ACCUMULATOR IS ZERO

The I-Register will contain the binary equivalent of the digit seven. 0111. I1 I2 I3 $\overline{\text{I4}}$ to give the instruction:- If the number in the accumulator is zero, proceed as Function 8. If not proceed sequentially.

This function proceeds to execute a test on the Accumulator taking place in two stages to determine its zero content. The first occurs at block 71 testing for a negative accumulator. The second test entered at Block 72B determines the existence of a positive Accumulator.

If the result of the summutation at Block 71 is not negative, the Accumulator may be zero, and if the 2's complement of the accumulator at Block 72B is not negative, the Jump instructions can be implemented in Block 73B.

The sequence commences at the resting point C2 and continues through C6B or C7 into Block 70. The operation may be followed in Figs. A11, A15 and A16.

15.1 Block 70

Transfer the address from the M-Register into the Q-Register.

MTF. The Valid address in the M-Register that is transferred to the adding unit.

F N
0.1110/001110000000

DTF_1 and DTF_2 is the collate constant.

$\overline{OTG}$ clears the G-Register.

VTG places 0.0000011100000000 into the G-Register

$\overline{OTG}$ clears the Q-Register.

GTQ places 0.0000011100000000 into the Auxiliary Register

15.2 Block 71

Transfer the contents of the A-Register into the M-Register then test for a negative M-Register.

ARF. The Accumulator contains 0.0000000000000000 and is transferred to the Adding Unit. The G-Register is cleared by $\overline{OTG}$.

FTG. Transfer 0.0000000000000000 into G. (G=0.0000000000000000)

$\overline{OTM}$ The M-Register is now cleared of its contents.

GTM Place the contents of the G-Register into the M-Register 0.0000000000000000 M = 0.0000000000000000).

TM18. This tests the M18 position by means of conditionals.

M18=0 Therefore the contents of A was not negative, therefore the matrix address generated transfers the operation to Block 72B.

If M18 - 1 the accumulator would contain a negative number and this operation would then be transferred to block 72A instead.

15.3 Block 72B

Change the M-Register to 2's complement of present contents, then test for negative M-Register.

$\overline{\text{MTF}}$ is the inverse output of the M-Register bistables to the Accumulator. This is 1.1111111111111111

$$1.\text{TF} \quad \frac{1}{10.0000000000000000}$$

The positive digit is out of range being in the position of bit 19.

$\overline{\text{OTG}}$. Clears the G-Register

RTG. Transfers the contents of the Adder into the G-Register. Place 0.0000000000000000 into G. (G=0.0000000000000000).

$\overline{\text{OTJ}}$. Clears the J-Register. $\overline{\text{OTM}}$ clears the M-Register.

GTM. Transfers the contents of the G-Register into the M-Register. Place 0.0000000000000000 into M. (M=0.0000000000000000).

TM18 tests the M18 position by means of conditionals.

M18=0. Therefore the contents of the Accumulator was zero and not a positive number. The matrix address generated is the address of Block 73B.

If M18=1, the Accumulator would then contain a positive number, and the operation would then be transferred to Block 73A instead.

15.4 Block 73B

Put the address of the SCR into the J-Register, then write the address from the Q-Register into that SCR.

QTF transfers the digital content of the Q-Register into the Adder.

F = 0.00000011100000000

ETJ. Place the address of the current SCR into the J-Register i.e. 0, 2, 4 or 6.

$\overline{\text{OTG}}$ Clear the G-Register.

FTG. Transfer the digital content of the Adder into the G-Register. Place 0.00000011100000000 into G (G=0.00000011100000000).

$\overline{\text{OTM}}$ Clear the M-Register.

GTM. Place the address N which is the digital content of G into the M-Register. This is the new JUMP address required for the FUNCTION 7.

CLEAR. Clear the former content of the SCR.

WRITE the new M-Register content which is the JUMP address into the store (SCR 0, 2, 4 or 6).

16. FUNCTION 8 JUMP

The I-Register will contain the binary equivalent of the digit eight which is 1000 or $\overline{I1}$, $\overline{I2}$, $\overline{I3}$, I4 to give the instruction: Place the N-digits of the instruction into the SCR. The next instruction to be obeyed will be the contents of the location specified by the N-digits.

The SCR is normally incremented by one each time an instruction is obeyed. Where it is required to access a location of a different address, a jump function may be specified. This will move the incremented address set-up during the previous instruction and replace it with the address to which the computer is required to Jump. The Control Sequence at C2 is implemented and the instructions enter Block 80.

16.1 Block 80

Set the J-Register with the address of the SCR.

$\overline{\text{OTJ}}$, ETJ. The J-Register is reset and ETJ sets up the J-Register with the SCR address from the E1 and E2 staticizers. The operation is transferred to Block 81. The drawings illustrating this Function are identical with Function 7.

16.2 Block 81

CLEAR. Clears the SCR. The Jump address is written in by WRITE to complete this Function.

17. FUNCTION 9. JUMP IF ACCUMULATOR IS NEGATIVE

The I-Register contains the binary equivalent of the digit 9, which is 1001, or I1, $\overline{\text{I2}}$, $\overline{\text{I3}}$, 14 to give the instruction: If the number in the Accumulator is negative, proceed as Function 8. If not negative, proceed sequentially. The control sequence is implemented and from C6 or C7 the matrix address generated initiates the operation in Block 90. The drawings illustrating this Function are identical with Function 7.

17.1 Block 90

Transfer the address from the M-Register into the Q-Register.

The incidence of the waveform MTF strobes the contents of the M-Register into the adding unit; The G-Register is reset and the address collated out by DTF_1, DTF_2, VTG enters the G-Register. The waveform $\overline{\text{OTQ}}$ resets the Auxiliary register and GTQ transfers the contents of the G-Register into the Q-Register. The matrix address for Block 91 is generated transferring the operation.

17.2 Block 91

Transfer the contents of the Accumulator to the M-Register, then test for a negative number in the M-Register. The waveforms ATF, FTG, GTM, place the Accumulator contents into the M-Register where the waveform TM18 tests for the presence of a sign digit. If the Accumulator is negative, M18=1 and the conditional gating signal originates a matrix address to transfer the operation to Block 92A.

17.3 Block 92A

Place the SCR address into the J-Register, then write address from the Q-Register into that SCR. ETJ. This waveform sets up the SCR address from the E-bistables. QTF. The address in the Auxiliary Register transferred to the Adding Unit. The G-Register is strobed by $\overline{\text{OTG}}$ clearing it, $\overline{\text{OTM}}$ clears the M-Register and GTM transfers the contents of the G-Register into the M-Register. The SCR is cleared and WRITE writes the new information into the SCR. The operation now being completed proceeds as Function 8.

17.4 Block 92B

If during the test for the presence of a sign digit, the Accumulator is positive, M18=0, the gating conditions at Block 50 will not be satisfied and the matrix address generated will transfer the operation to Block 92B and back to the quiescent point C2.

18. FUNCTION 10. COUNT IN STORE

The I-Register will contain the binary equivalent of the digit ten which in four bits is 1010 or $\overline{\text{I1}}$, I2, $\overline{\text{I3}}$, I4 to give the instruction: Add 2^{-17} to the number in the store location specified.

The operation commences at the quiescent point C2, and either to C6B or C7 and to Block 100. The operation can be followed using the identical drawings for Function 2.

18.1 Block 100

Transfer the address from the M-Register into the J-Register, then read the number from that address into the M-Register. READ. This waveform results in the store location being cleared. The matrix address generated transfers the operation to Block 101.

18.2 Block 101

Increase the number in the M-Register by 1, then write the increased number back into the store.

MTF, 1.TF. The contents of the M-Register is transferred to the Adding Unit, and 2^{-17} is added by the waveform 1.TF. This places a '1' in the least significant digit position of the Adding Unit and the resulting sum transferred to the G-Register by $\overline{\text{OTM}}$, GTM. This is written back into the addressed location by WRITE. The sequence returns to the quiescent point at C2.

19. FUNCTION 11. STORE SCR

The I-Register will contain the binary equivalent of the digit 11, 1011 or I1, I2, $\overline{\text{I3}}$, I4 to give the instruction: Store bits 1-13 of the SCR (relative to the current program level) in the Store location specified and bits 14-18 of the SCR transferred to the Q-register.

The operation commences at the quiescent point C2 beginning the control sequence. The matrix address of Block 110 is generated. The operation may be followed using identical drawings for Function 2.

19.1 Block 110

Transfer address of storage location from the M-Register into the Q-Register and set the J-Register with the address of the SCR then read the contents of the SCR into the M-Register.

MTF transfers the contents of the M-Register into the Adding Unit which is the valid address. DTF1 and DTF2 are the collate constants. VTG. ETJ, the address of the current SCR is placed into the J-Register. $\overline{\text{OTG}}$, VTG clear the G-Register and collate out all digits in the adder and place them into the G-Register. $\overline{\text{OTQ}}$ clears the Auxiliary Register and GTQ transfers the address from the G-Register to the Q-Register. $\overline{\text{OTM}}$ clears the M-Register. READ accesses the location specified and places the contents of the SCR into the M-Register. WRITE. The new information is written back into the store. The matrix address generated transfers the operation to Block 111.

19.2 Block 111

The address is transferred from the Q-Register by QTF and FTG into the G-Register.

The waveforms $\overline{\text{OTG}}$ and $\overline{\text{OTJ}}$ clear their pertinent registers at the appropriate times. With GTJ, the instruction N digits are placed into the J-Register to provide the address of the location into which the SCR content is to be stored.

19.3 Block 112

With these micro-instructions bits 14-18 of the SCR are placed into Q by MTF, DTF2, $\overline{\text{OTG}}$, VTG, $\overline{\text{OTQ}}$ and GTQ.

19.4 Block 113

The waveforms MTF, DTF1, $\overline{\text{OTG}}$, VTG, $\overline{\text{OTM}}$, GTM clear the five most significant digits out of the M-Register. CLEAR. Clears the store location specified. WRITE writes the M-Register contents into the address specified. The control sequence returns to the quiescent point at C2.

20. FUNCTION 12. MULTIPLY

The I-Register will contain the binary equivalent of the number 12 which is 1100 or $\overline{\text{I1}}$, $\overline{\text{I2}}$, I3, I4 to give the instruction. Multiply the number in the Accumulator by the number in the Store location specified. Place the result into the Accumulator and Auxiliary Registers.

The individual stages of a multiplication consist of a closed loop in which the instructions add, subtract, and shift one place to the right, are consummated in accordance with the conditionals corresponding to the rules of binary multiplication given in the text.

The rules of multiplication may be expressed in the following manner:

Beginning at the point of the least significant digit, and assuming the less significant digit to be '0', inspect at each stage the corresponding digit of the multiplicand together with the neighbouring less significant digit. The relationship between these digits determines the use to be made of the multiplier. With the exception of the sign digit, each digit in the multiplicand is thus examined twice.

Rule 1. If the given multiplicand-digit is one, and the less significant digit zero, subtract the multiplier from the partial product, which was initially zero.

Rule 2. If the multiplicand-digit is zero, and the less significant digit is one, add the multiplier to the partial product.

Rule 3. If both digits are alike, do nothing.

The multiplicand, which is also held in the Q-Register is right shifted one place at each stage of multiplication, eventually going out of range. Thus by examining the digit in the Q1 position and the content of the Overflow Unit at each stage, the relationship between the multiplicand digits may be determined. (Where Q. 1 holds the digit of greater significance of the pair being examined).

On completion of a multiplicand operation, the accumulator holds the 17 most significant digits of the product and the Q-Register the 17 least significant digits.

The logic elements that comprise the matrix are located on the board 14/A-GF. The logic circuits delineating the operation may be followed in Figs A10, A11 and A16.

The control sequence begins at C2 through C6 or C7 setting-up the matrix address of Block 120.

20.1 Block 120

Commencing at the first stage of Function 12, the micro-program proceeds as follows:

The address of the multiplier is transferred to the Adding Unit by MTF.

$\overline{\text{OTG}}$, FTG, OTM, GTJ. These waveforms clear the G and M-Registers and transfers the address of the multiplier to the J-Register. READ/WRITE. The M-Register is cleared and the contents of the J-Register read into the M-Register. The termination of the micro-instruction generates a matrix address and the operation proceeds to Block 121.

20.2 Block 121

ATF, $\overline{\text{OTG}}$, FTG, $\overline{\text{OTA}}$, OTQ, GTQ. These waveforms clear the G, A and Q-registers. The multiplicand is placed into the Auxiliary Register.

$\overline{\text{OTJ}}$, $\overline{\text{OTX}}$, KTJ, JTPC. The J-Register is cleared and set-up to 17, the X-bistable is set to zero. TXQ1 compares X with Q1. $\overline{\text{OTA}}$ clears the accumulator. The Q-Register now holds the more significant digit of the multiplicand pair in the first digit position (Q1), the X-bistable (Overflow Unit) holds the lesser multiplicand digit. Thus X.Q1 (Q1 = 0, X = 1) would give the multiplicand digit relationship 01 add, permitting the multiplier to be added into the accumulator. X.Q1 (Q.1 = 1, X = 0) therefore would give the condition 10 and the multiplier is negated and added into the Accumulator when X $\equiv$ Q1, it gives the conditions '11' or '00' and nothing is added to the Accumulator.

Both the multiplier (which has been held in the M-Register throughout the process of computation) and the partial product undergo processing as determined by the conditionals originating in Blocks 121 and 124. These reiterate the rules of multiplication. The operations in Block 121 give rise to conditionals transferring the operation to Block 122. In this block there is a two-way choice since X = 0 i.e. X $\equiv$ Q1, $\overline{\text{X}}$.Q1. Assuming that conditions are not satisfied for $\overline{\text{X}}$.Q1, but are for X $\equiv$ Q1, then the address of the block selected to continue the computations will be that of Block 122C.

20.3 Block 122C

The multiplicand in the Accumulator is transferred to the Adding Unit and shifted one place to the Right then replaced into the Accumulator by the waveforms ATF, $\overline{\text{OTG}}$, RTG, $\overline{\text{OTA}}$, GTA. The

Overflow Register is gated setting the X-bistable for detection of an overflow digit by RTG and YTX. The Accumulator and X-bistable are cleared by $\overline{\text{OTA}}$ and $\overline{\text{OTX}}$ immediately before being set with the new information. With 1TPC the count in the Process Counter is decreased by one. The micro-instructions continue the operation in Block 124.

20.4 Block 124

The multiplicand is held in the Q-Register and right-shifted one place at each stage of multiplication, eventually going out of range. This operation is implemented by QTF, $\overline{\text{OTG}}$, RTG, $\overline{\text{OTQ}}$, GTQ.

An examination of the digit in Q1 and the content of the overflow unit at each stage gives the relationship between the multiplicand digits TPCO, TXQ1.

The Process Counter is tested for zero and X is compared with Q1. If $C \neq 0$, the conditionals implement a recycling in the determination as to the conditions that satisfy the choice between $X \equiv Q1$, $\overline{X}.Q1$, $X.\overline{Q1}$ in Block 122. If $C = 0$ the operation is transferred to Block 123. If conditions are not satisfied for $X \equiv Q1$ and $\overline{X} = Q1$ but are for $X\overline{Q1}$, the address of Block 123A will be generated.

20.5 Block 123A

The multiplication process is completed in block 123. The rise of ATF and MTF transfers the partial product and the multiplier into the Adding Unit. The G-Register is cleared and the output of the Adding Unit is transferred to the G-Register. As the Accumulator is cleared of its former contents, the X-bistable is set to zero. The finalised product is gated into the Accumulator and the operation now returns to the quiescent point. The Q-Register now contains the 17 least significant digits of the product.

20.6 Blocks 122A, 122B, 123B, 123C

These four blocks may be entered depending upon the conditionals and the operations carried out in these blocks may be seen by referring to Fig. A12.

Worked Example

Multiply $(+\frac{11}{16})$ x $(+\frac{13}{16})$ the binary equivalent of which is 0.1011 by 0.1101, and disregard the thirteen remaining cyphers in the computer word length. The operation commences at Block 120 of the Control Sequence where the multiplier is read from the store into the M-Register.

BLOCK 120, 121

READ/WRITE	M = 0.1101
$\overline{\text{OTG}}$	G = 0.0000
ATF, FTG	G = 0.1011
GTQ	Q = 0.1011
KTJ. JTPC	J = Count = 4
$\overline{\text{OTA}}$	A = 0.0000
$\overline{\text{OTX}}$	X = 0

TXQ1 X = 0, Q1 = 1 By rule 1. Subtract

Which satisfies $\overline{X}.Q1$ block 122B

BLOCK 122B, 124

ATF		0.0000	
$\overline{\text{MTF}}$		1.0010	
1.TF		$\frac{1}{1.0011}$	
RTG	G =	1.1001	Y = 1
YTX			X = 1

GTA	A = 1.1001	
QTF	0.1011	
XTF	1	
RTG	1.0101	Y = 1
GTQ, YTX	Q = 1.0101	X = 1

Q18 now contains the first digit of the product.

1TPC	Count = 3
TPC0	Test for zero shows positive result.
TXQ1	X = 1 Q1 = 1 By Rule 3. Do nothing

Conditions are satisfied for X = Q1 block 122C.

BLOCK 122C. 124.

ATF	1.1001	
RTG	G = 1.1100	Y = 1
YTX, GTA	A = 1.1100	X = 1
QTF	1.0101	
XTF	1	
RTG	1.1010	Y = 1
GTQ, YTX	Q = 1.1010	X = 1

Q18, Q17 are the two least significant digits of product.

1TPC	Count = 2
TPC0	Test Process Counter for zero shows positive.
TXQ1	X = 1, Q.1 = 0. From Rule 2. Add.

Which satisfies $X.\overline{Q1}$ block 122A.

BLOCK 122A. 124

ATF	1.1100
MTF	0.1101
	0.1001

RTG		1.0100	Y = 1
GTA, YTX	A =	0.0100	X = 1
QTF		1.1010	
XTF		1	
RTG		1.1101	Y = 0
GTQ, YTX	Q =	1.1101	X = 0

Q18, Q17, Q16 hold least three significant digits of product.

1TPC Count = 1

TPC0 Test Process Counter for zero shows positive.

TXQ1 X = 0, Q.1 = 1. By Rule 1. Subtract.

Which satisfies $\overline{X}$.Q1 block 122B.

BLOCK 122B. 124

ATF		0.0100	
$\overline{M}$TF		1.0010	
1.TF		1	
		1.0111	
RTG		1.1011	Y = 1
GTA, YTX	A =	1.1011	X = 1
QTF		1.1101	
XTF		1	
RTG		1.1110	Y = 1
GTQ, YTX	Q =	1.1110	X = 1

Q18, Q17, Q16, Q15 hold the four least significant digits of product.

1TPC Count = 0

TPC0 Test process counter for zero shows negative

TXQ1 X = 1 Q.1 = 0. By rule 2 Add.

Which satisfies X.$\overline{Q1}$ block 123A

BLOCK 123A

ATF		1.1011
MTF		0.1101
FTG		0.1000
GTA	A =	0.1000

Q = 1.1110 which means the product 0.100011110

which is

$$+\frac{143}{256}$$

The Q-Register is accessed separately by Function 3.

20.7 Mathematical Justification

Let M be the multiplicand and Q be the multiplier.

Then if the least significant digits are q1, q2, q3 ----------

q18 (sign), the successive partial products are formed as follows:-

$$P_1 = -\tfrac{1}{2}q_1 . M.$$

$$P_2 = \tfrac{1}{2}\left[P_1 + (q_1 - q_2)\, M\right].$$

$$P_{n+1} = \tfrac{1}{2}\left[P_n + (q_n - q_{n+1})\, M\right].$$

P_{n+1} can be expressed as the following:-

$$M\left[\tfrac{1}{2}(q_n - q_{n+1}) + \tfrac{1}{4}(q_{n-1} - q_n) + \tfrac{1}{8}(q_{n-2} - q_{n-1}) \ldots\ldots\ldots\ldots \right.$$

$$\left. \ldots\ldots + \tfrac{1}{2}n(q_1 - q_2) - \frac{1}{2n+1}\, q_1\right].$$

$$= M\left[-\tfrac{1}{2}q_{n+1} + \tfrac{1}{4}q_n + \tfrac{1}{8}q_{n-1} + \tfrac{1}{2}nq_2 + \frac{1}{2n+1}\, q_1\right].$$

The last partial product formed in this way is P_{17} which is:-

$$P_{17} = M(-\tfrac{1}{2}q_{17} + \tfrac{1}{4}q_{16} \text{ ---------- } + 2^{-17}q_1).$$

The final product is obtained by:-

$$P_{18} = P_{17} + (q_{17} - q_{18})M.$$
$$= M(-q_{18} + \tfrac{1}{2}q_{17} + \tfrac{1}{4}q_{16} \text{ ---------- } +2^{-17}q_1).$$

As q_1 to q_{18} are the binary digits of Q, we have:-

$$-q_{18} + \tfrac{1}{2}q_{17} + \tfrac{1}{4}q_{16} \text{ ---------- } +2^{-17}q_1 = Q.$$

Thus $P_{18} = MQ$.

Therefore the process constitutes the exact product of M and Q, with the exception where M and Q are equal to -1.0. In this case however, the product is out of range.

21. FUNCTION 13. DIVIDE

The I-Register will contain 1101, the binary equivalent of 13 or I1, $\overline{I2}$, I3, I4 to give the following instruction:- Divide the number in the Accumulator and Auxiliary Register by the number in the specified store location, placing the Quotient in the Accumulator.

The rules of division may be expressed in the following manner:-

(i) Compare the sign digits of divisor and dividend (or remainder). If of like sign, subtract divisor from dividend and add 1 into the quotient. If the digits are not of like sign, add divisor to dividend and add 0 into the quotient.

(ii) Multiply the remainder by two and return to step (i). This procedure is repeated an additional 17 times to determine successive digits of the quotient. These are placed into the answer occupying positions of descending order of significance.

(iii) The remaining digit of the quotient is made equal to 1. The first digit placed into the answer is disregarded.

Initially the dividend (double length) is held in the Accumulator and the 17 most significant digits of Q and the divisor in M.

The preliminary steps include transferring the address from the M-Register into the J-Register followed by reading that address into the M-Register as detailed in Block 130. Clearing the least significant digit of Q is accomplished by shifting Q one place to the Right as in block 131, then one place to the left as in block 132 and setting-up both the J-Register and Process Counter to 18. One essential of the division operation is shifting the A-Register one place to the left during the transfer into the G-Register, as shown in block 133. The test TXM18 determines the future path of the Control Sequence of the division cycle in blocks 134 and 136.

During the division process, the quotient takes form, digit by digit in the Q-Register during each cycle, as the least significant part of the dividend is shifted into the Accumulator by the repeated doubling of the remainder. Comparison of remainder and dividend signs occur in block 136, where the M-Register is added to or subtracted from the A-Register, then left-shifted one place with X0 added. The result is placed into the Accumulator. The X-bistable is set with the overflow and the Process Counter is tested for zero. Comparison between the remainder and the dividend occurs by setting the TXM18 conditional on X and M18. If PC=0, the microprogram enters block 135.

The termination of the division operation occurs in block 135 where the quotient assembled in Q has the digit one added by 1. TF in its least significant position and the resulting rounded quotient placed in A. The digit placed in Q as a result of the initial comparison of signs

does not appear in the final quotient as it is shifted out at the final comparison stage. The remainder is not utilized.

The logic of the operation can be followed in the Figs. A10, A12 and A16.

The foregoing procedure is exemplified by a worked out problem elucidating the conditions formulated by the Control Sequence. A simplified process is given using seven bit word lengths and a synthesized count of 7.

Commencing at Block 130. The micro-instructions addressed by these waveforms (GTJ - READ WRITE) in Block 130 place the N-digits of the instruction into the J-Register and read the divisor from the addressed store location. The dividend was placed in the Accumulator and Auxiliary Register by a previous instruction.

The count instruction is set-up to 18 in block 132 for division by K2 and KTJ in the J-Register and by JTPC in the Process Counter. By placing 18 in the J-Register with KTJ, the count instruction governs the number of times in which the minor loops comprising the division operation is recycled.

The control sequence shows that 1TPC reduces the count of the Process Counter by 1 each time the minor loop is recycled.

The completion of the 18th cycle will leave the Process Counter with zero content. Commencement of the 18th stage promote the conditions necessary to leave the minor loop and round off the resultant quotient. Rounding-off occurs at block 135 (QTF, 1.TF, FTG, GTA). The quotient is contained in the auxiliary register at this point and the round-off digit 1.TF is added.

21.1 Worked Example

Set the accumulator to ($+\frac{27}{64}$) binary 0.011011, the selected store location to ($+\frac{9}{16}$) binary 0.100100 and the auxiliary register to zero. The steps taken in the division will be as follows:

Block	Micro Instructions	Conditionals CA	Conditionals $\overline{CA}$	O/F Y	Bistables X	Bistables R	Digit Position Content
							7 5 3 1 A=0.011011($+\frac{27}{64}$)
130	GTJ READ/WRITE					M	0.100100 M=0.100100($+\frac{9}{16}$)
131	QTF						0.000000
	RTG			0		G	0.000000
	GTQ					Q	0.000000
132	QTF						0.000000
	LTG			0		G	0.000000
	GTQ					Q	0.000000
	KTJ,K2,JTPC) Count set of 7)					J	0111 Count = 7
133	ATF						0.011011
	YTX				0		
	LTG			0		G	0.001101
	TXM18	0	1	Which satisfies conditions for Block 134B			
134B	QTF						0.000000 The digit is high-lighted
	1.TF						1 (the first quotient digit is ultimately disregarded)

Block	Micro Instructions	Conditionals CA	Conditionals $\overline{CA}$	O/F Y	Bistables X	Bistables R	Digit Position Content 7 5 3 1	
134B	LTG			0		G	0.000010	Digits appearing in positions of lower significance are the most significant digits of the quotient.
	YTX				0			
	GTQ					Q	0.000010	
	1TPC						Count = 6	
	CRS	0	1					
136B	ATF						0.011011	
	$\overline{M}$TF						1.011011	
	1.TF						1	
							1.110111	
	XTF LTG			1		G	1.101110	
	GTA YTX				1	A	1.101110	
	TPC0	Test count for zero and selects Block 134						
	TXM18	1	0	Which satisfies conditions for Block 134A				
134A	QTF						0.000010	
	LTG			0		G	0.000100	
	YTX				0			
	GTQ					Q	0.000100	
	1TPC							Count = 5
	CRS	1	0					
136A	ATF						1.101110	
	MTF						0.100100	
							0.010010	
	XTF, LTG			0		G	0.100100	
	YTX, GTA				0	A	0.100100	
	TPC0	Test count for zero and selects Block 134						
	TXM18	0	1	Which satisfies conditions for Block 134B				

Block	Micro Instructions	Conditionals CA	Conditionals $\overline{CA}$	O/F Bistables Y	X	R	Digit Position Content 7 5 3 1
134B	QTF						0.000100
	1.TF						1
							0.000101
	LTG			0		G	0.001010
	GTQ, YTX				0	Q	0.001010
	1TPC						Count = 4
	CRS	0	1				
136B	ATF						0.100100
	$\overline{MTF}$						1.011011
	1.TF						1
							0.000000
	XTF, LTG			0		G	0.000000
	YTX, GTA				0	A	0.000000
	TPC0	Test count for zero and selects Block 134					
	TXM18	0	1	Which satisfies conditions for Block 134B			
134B	QTF						0.001010
	1.TF						1
							0.001011
	LTG			0		G	0.010110
	GTQ, YTX				0	Q	0.010110
	1TPC						Count = 3
	CRS	0	1				
136B	ATF						0.000000
	$\overline{MTF}$						1.011011
	1.TF						1
							1.011100

Block	Micro Instructions	Conditionals CA	Conditionals $\overline{CA}$	O/F Y	Bistables X	Bistables R	Digit Position Content 7 5 3 1
136B	XTF, LTG			1		G	0.111000
	YTX, GTA				1	A	0.111000
	TPC0	Test count for zero and selects Block 134					
	TXM18	1	0	Which satisfies conditions for Block 134A			
134A	QTF						0.010110
	LTG			0		G	0.101100
	YTX, GTQ				0	Q	0.101100
	1TPC						Count = 2
	CRS	1	0				
136A	ATF						0.111000
	MTF						0.100100
							1.011100
	XTF, LTG			1		G	0.111000
	YTX, GTA				1	A	0.111000
	TPC0	Test count for zero and selects block 134					
	TXM18	1	0	Satisfying conditions for Block 134A			
134A	QTF						0.101100
	LTQ			0		G	1.011000
	YTX, GTQ				0	Q	1.011000
	1TPC						
	CRS	1	0				Count = 1
136A	ATF						0.111000
	MTF						0.100100
							1.011100

Block	Micro Instructions	Conditionals CA	Conditionals $\overline{CA}$	O/F Bistables Y	O/F Bistables X	O/F Bistables R	Digit Position Content 7 5 3 1
136A	XTF, LTG			1		G	0.111000
	YTX, GTA				1	A	0.111000
	TPC0	Test count for zero and selects Block 134					
	TXM18	1	0	Satisfying conditions for Block 134A			
134A	QTF						1.011000
	LTG			1		G	0.110000
	YTX, GTQ				1	Q	0.110000
	1TPC						Count = 0
	CRS	1	0				
136A	ATF						0.111000
	MTF						0.100100
							1.011100
	XTF, LTG			1		G	0.111001
	YTX, GTA				1	A	0.111001
	TPC0	Test count for zero and selects Block 135					
	PC=0	Satisfies conditions to enter Block 135					
135	QTF						0.110000
	1.TF						1 Round off digit
	FTG					G	0.110001
	GTA					A	0.110001
							$= (+\frac{3}{4} + \frac{1}{64}) = \frac{49}{64}$

21.2 Mathematical Justification of the Process of Division

Let the binary digit placed in the quotient at the rth stage be qr, then the remainder following this stage R_r can be expressed in terms of the previous remainder as follows:-

$$R_r = 2\left[R_{r-1} + (1-2q_r)\ D\right] \quad \ldots\ldots 1.$$

In the preliminary stage we calculate,

$$R_1 = 2\left[N + (1 - 2q_1)\ D\right] \quad \ldots\ldots 2.$$

Thus after n stages we can write

$$R_n = 2(1-2q_n)\ D + 4(1-2q_{n-1})\ D + 8(1-2q_{n-2})D \ldots + 2^n(1-2q_1)D + 2^n.N \ldots 3.$$

$$= (2+4+8+16.\ldots.2^n)D + 2^n.N - (4q_n + 8q_{n-1}\ldots.2^nq_2 + 2^{n+1}q_1)D \ldots. 4.$$

The quotient produced after 18 comparisons is used, so that we can substitute n=18 in the above formula. The unrounded quotient we generate becomes

$$Q = -q_2 + 2^{-1}q_3 + 2^{-2}q_4 \ldots\ldots 2^{-16}q_{18} \quad \ldots\ldots 5.$$

thus

$$R_{18} = (2+4+8+16.\ldots.2^{18})D + 2^{18}N - 2^{18}(2^{-16}q_{18} + 2^{-15}q_{17} \ldots + 2^{-1}q_3 + q_2 + 2q_1)D \ldots. 6.$$

$$= (2+4+8+16.\ldots.2^{18})D + 2^{18}N - 2^{18}(Q + 2q_2 + 2q_1)\ D \quad \ldots\ldots 7.$$

$$= (2^{19} - 2)D + 2^{18}N - 2^{18}\ QD - 2^{19}(q_2 + q_1)D \quad \ldots\ldots 8.$$

∴ Rearranging as an expression for Q

$$Q = \frac{N}{D} + \frac{(2^{19} - 2)}{(2^{18})} - 2\ (q2 + q1) - 2^{-18}\ \frac{R_{18}}{D} \quad \ldots\ldots 9.$$

To show that Q is approximately the correct quotient, it is now necessary to establish the size of q_2, q_1 and R_{18}.

Consider the formation of R_1 under four conditions.

(1) N and D are positive.

If the quotient is within the computers normal range of numbers, then we have $D > N \geqslant 0$ i.e. $0 > N - D \geqslant -D$

Therefore in this case $R_1 = 2(N-D)$ is negative.

(2) N and D are negative.

Then $0 > N > D \geqslant -1$ i.e. $-D > N - D > 0$

Therefore R_1 is positive

(3) N is positive and D is negative

now $-D \geqslant N \geqslant 0$

Therefore $0 \geqslant N + D \geqslant D$

i.e. R_1 is negative unless $N = -D$

(This special case is dealt with later)

(4) N is negative, D is positive

$0 > N \geqslant -D$

Therefore $D > N + D \geqslant 0$

i.e. R_1 is positive

Generally then R_1 is opposite in sign to N; this implies that when q_1 is 0, q_2 is 1 and vice versa [as $q_1 = 1$ if (sign N = sign D) and $q_2 = 1$ if (sign R_1 = sign D)] so in the above expression for Q we can substitute $q_1 + q_2 = 1$ resulting in

$$Q = \frac{N}{D} - 2^{-17} - 2^{-18} \frac{R_{18}}{D} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 10.$$

The above inequalities show that, neglecting special cases, $|R_1| < 2|D|$. A similar set of inequalities can then be obtained showing that $|R_2| < 2|D|$ and from this it can be deduced that all the R's be within the same limits so that the last term in the expression for Q has

a maximum range of $\pm 2^{-17}$.

so that $Q = \frac{N}{D} - 2^{-17} \pm 2^{-17}$ ..... 11.

Q is here the unrounded quotient, the rounding process which always adds 2^{-17} removes the "bias" so Q is correct to $\pm 2^{-17}$ i.e. is correct to 17 binary digits.

Further Notes

(1) The special case N = -D.

In this case R_1 has the same sign as N which normally means that the quotient is out of range. Since N and R_1 are both positive q_1 and q_2 are both 1. The term $-2(q_2 + q_1)$ in the expression for Q has a value of 4 so that Q is apparently 2 less than the correct result. Since Q is only available module 2, the calculated quotient will be correct.

(2) It will be realized that the result $|R_1| < 2|D|$ imples that R_1 (and subsequent R's) will be in the range $+2 > R \geqslant -2$ apparently requiring a 19 digit register and adder to deal with it. Addition over 19 digits is not, however necessary, as the summutation (or subtraction) before doubling, is in the range $1 > X \geqslant -1$ so that the 2^0 digit of this number (which appears in the usual sign digit position of the Adder) will be the same as its sign digit (in the 2^1 position).

The "sign" digit thereby generated is recorded in the X bistable for the next comparison but is not otherwise used.

22. FUNCTION 14. SHIFT. 14A. BLOCK TRANSFER

The I-Register contains the digits 1110, the binary form of the numeral 14 or $\overline{I}$. 1, I. 2, I. 3 and I. 4 to give the instruction:- Shift the number in the Accumulator and Auxiliary Register a number of places left

or right. If the two most significant N digits are 0 the number is shifted to the left by the number of places given in the address. Where the two most significant N digits are one, the Accumulator and Auxiliary Registers are right shifted or halved. For a right shift the number of places shifted is obtained by subtracting the address from 8, 192.

If the most significant N-digits is 0, and the next most significant is 1, then a block transfer input is carried out.

If the most significant N-digit is 1 and the next most significant digit is 0, then a block transfer output is carried out.

In each case the N-digits in the M-Register are the peripheral address and the contents of the Q-Register determine the number of words to be transferred. The A-register contains the address from which the transfer starts.

The entrance to Function 14 implements a comparison between M12 and M13 in Block 140 of the Control Sequence which may be seen in Fig. A12 and Fig. E.

The test TM12M13 and TM13 in block 140 determine which of the following operations are to be executed:

(i) FUNCTION 14. Block 142A if M12=M13=1. A right shift.

(ii) FUNCTION 14. Block 142B if M12=M13=0. A left shift.

(iii) FUNCTION 14A. Block 14A2 if M12 $\neq$ M13. A block transfer.

The logic operation to determine Block Transfer is initiated on the DE Conditional board 6A-F1 may be deduced from the drawing Fig. A16.

The conditionals CD and CE are the direct and inverse outputs of the same staticizer and are used to determine if a block transfer or a shift is to be carried out.

The staticizer is reset so that CD becomes true when SFD is strobed by t1. During Block 140, if M12=M13, then at t2 time the staticizer will be set so that CD is true indicating a shift function. If M12 ≠ M13, then the staticizer will remain with CE true indicating a block transfer.

In Block 140, if a shift is specified the waveform TM13 determines if a right or left shift is to be carried out. If M13=1 and the conditional CA is set it indicates a right shift. If M13=0 then the conditional $\overline{CA}$ is set indicating a left shift. These conditions may be seen in logic drawing A16.

22.1 Left Shift Right Shift

The contents of the Accumulator and Auxiliary Register are shifted by means of a FUNCTION 14. See Figs. f, g and h.

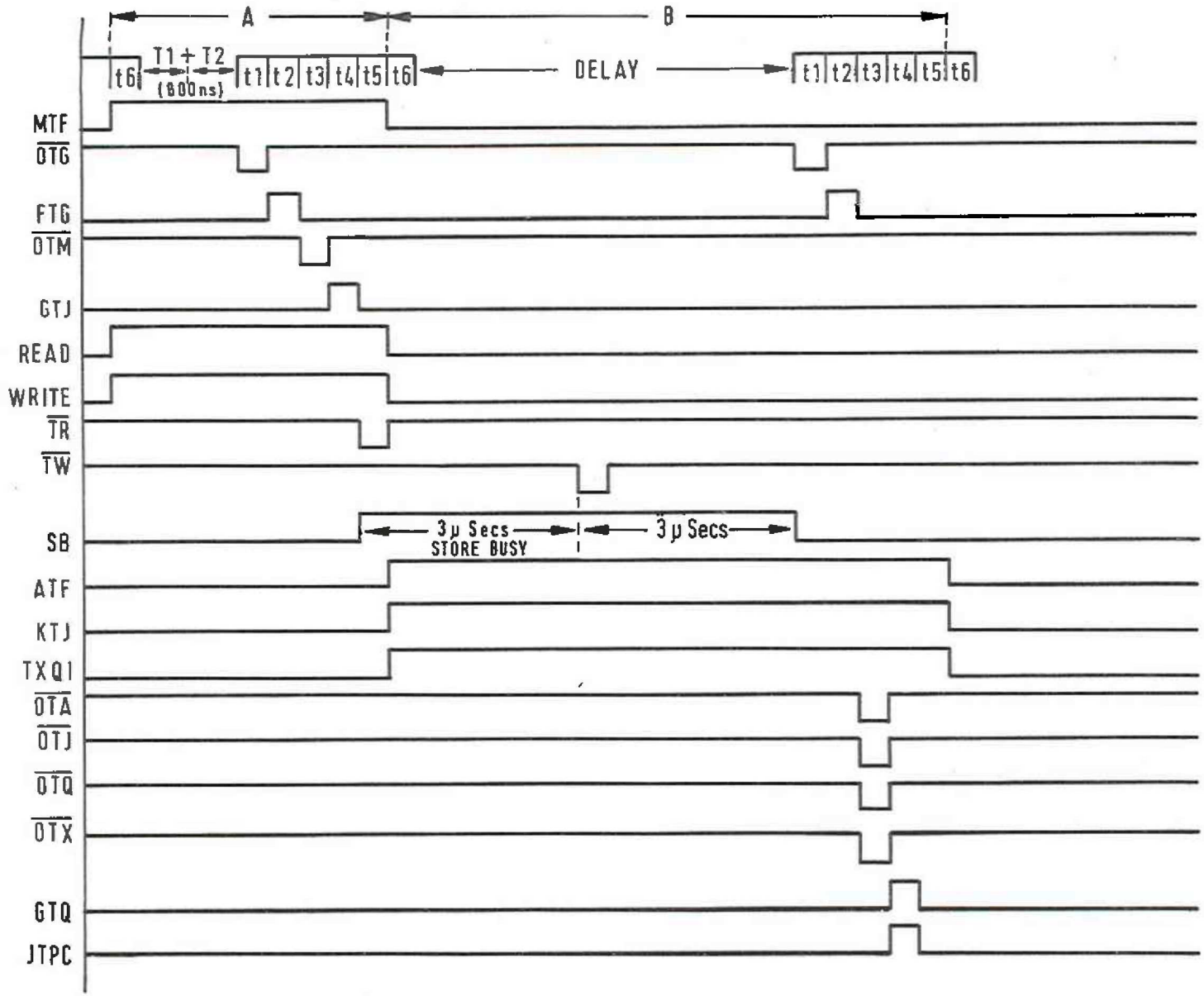
The logic for FUNCTION 14 is designed to place the N-digits of the shift instruction into the J and M Registers so that the number of places to be shifted may be ascertained and used to set up the Process Counter.

Where the Accumulator is to be shifted to the right, the M-Register is used to negate the N digits and enable subtraction from 8,192. In negated form, the N digits are reduced in steps of -2^{-17} with each shift of one digit position. The concept of subtracting from 8,192 is more readily visualised with reference to the following:

The M-Register is assumed to contain the address:

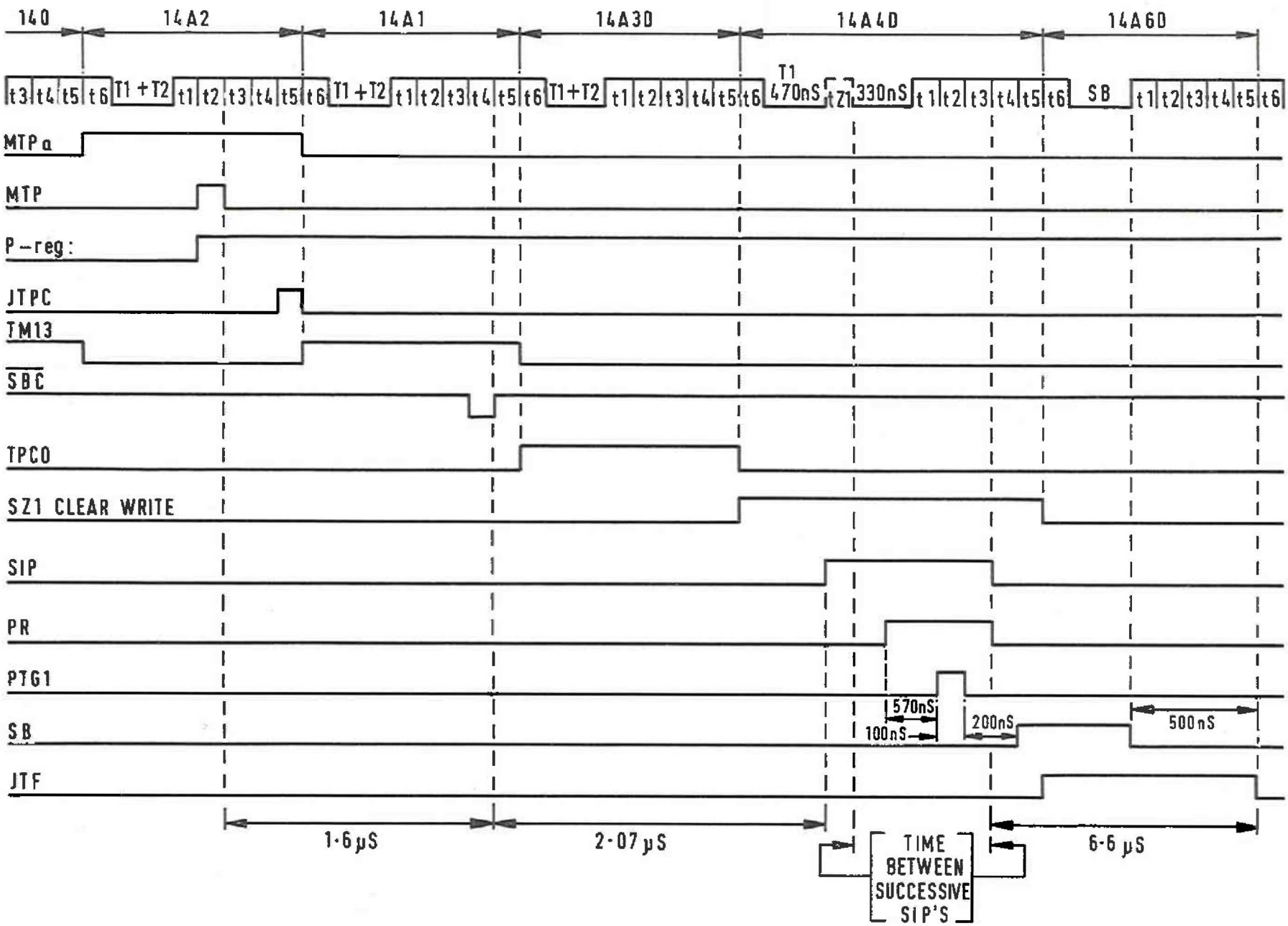
N

1111111111111 (N = 8191) which constitutes an order to shift the Accumulator one place to the right. Negating gives



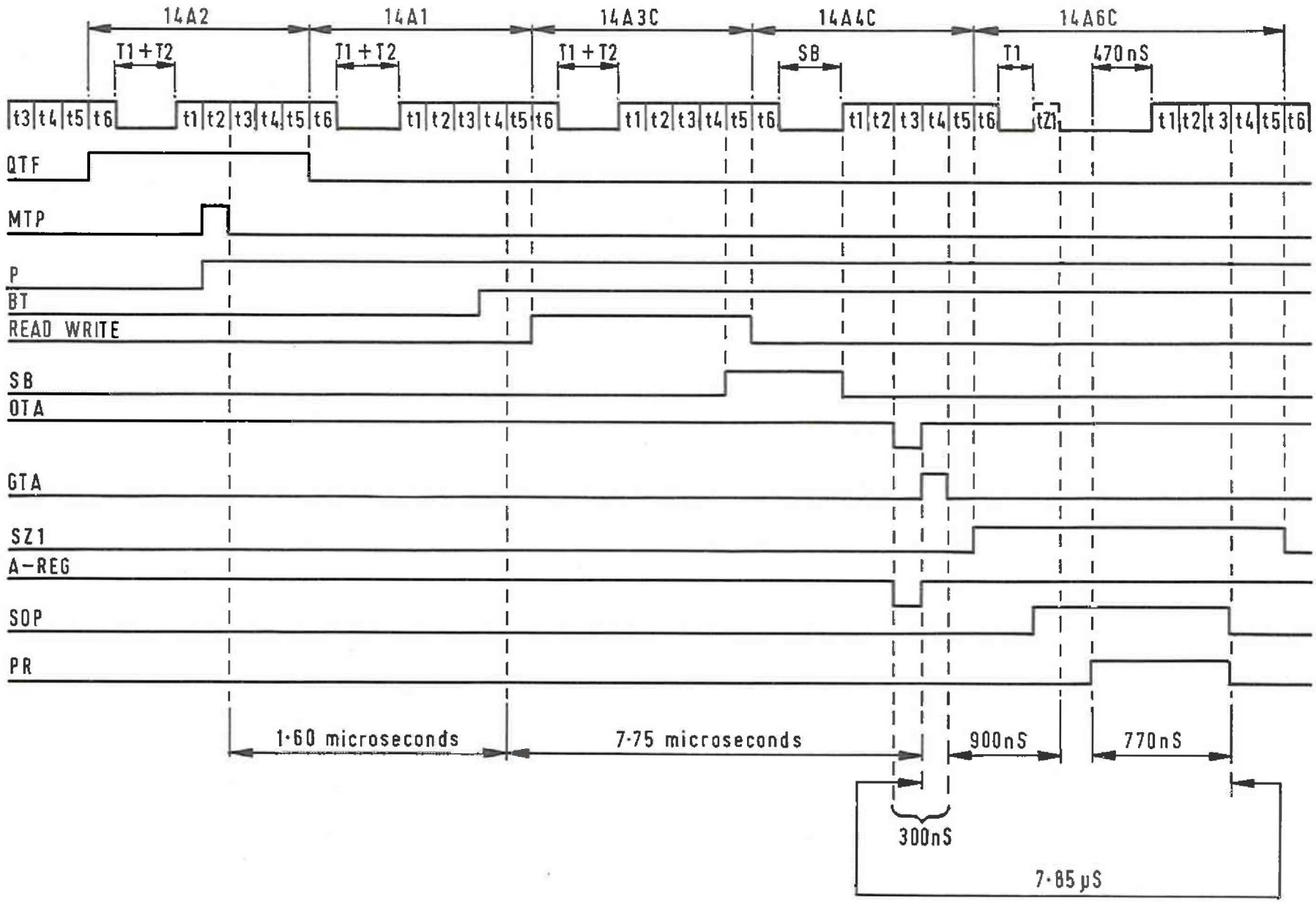
ISS 1.

FIG f. Typical control sequence waveforms and timing pulses.



ISS 1.

FIG g. Block Input function 14



ISS 1.

FIG.h. Block Output function 14

$\overline{\text{MTF}}$ 0000000000000

1.TF 1

FTG 0000000000001 which is the number of places to be shifted.

The count is set by placing the negated instruction N-digits into the J-Register. The Process Counter is thus set-up and control is exercised over the minor loop of blocks, 144A and 146A decrementing the PC count by one for every cycle and testing the P.C. for zero.

Note the action of the Overflow Unit bistables (Y and X) during the shift operation. Dependent on if shifts to the left or right are being executed, the least significant digits of the Accumulator will be placed into the overflow bistables and thence transferred into the most significant digit positions of the Auxiliary Register (Right Shifts). Alternatively, the most significant digits of the Auxiliary Register will be placed into the least significant digit positions of the Accumulator (Left Shifts).

Right shifting a positive number n places is equivalent to dividing the original number by 2n. That is if the Accumulator is set to 0.1000 ($+\frac{1}{2}$) a right shift of one place will give 0.0100 ($+\frac{1}{4}$) successive right shifts giving 0.0010 ($+\frac{1}{8}$) and 0.0001 ($+\frac{1}{16}$) respectively. The sign digit will remain unaffected.

Right shifting a negative number follows a similar pattern as shown by example. 1.100 ($-\frac{1}{2}$), 1.110 ($-\frac{1}{4}$), 1.111 ($-\frac{1}{8}$) etc.,

The converse applies when shifting n places left, which is equivalent to multiplying the original number by 2n.

An example of Left Shift is shown in Sec. 22.3 and of Right Shift in Sec. 22.4.

22.2 Block Transfer 14A

If a block transfer is indicated, the Control Sequence enters block 14A2. The micro-instructions select the peripheral, and JTPC sets-up the Process Counter with a count equal to the number in the Q-Register. Block 14A1 is now entered and ATF, FTG, GTJ transfers the address into the J-Register. The TM13 test determines if M13 = 0 or M13 = 1. As an example, if M13 = 1, the micro-instructions of block 14A3C perform TPC0, the zero test of the Process Counter and also read the contents of the store location specified into the M-Register. If PC = 0, the block 14A5 is entered and the sequence returns to the computer quiescent point at block C2. If PC $\neq$ 0 the sequence enters block 14A4C where the contents of the M-Register is transferred to the Accumulator. In block 14A6C. SZ1, WFP selects the peripheral and waits for a reply. JTF, 1.TF, FTG, GTJ, the address in the J-Register is incremented by one and 1TPC decrements the PC count by one. Exit from 14A6C is into block 14A3C again. This cycle is continued until PC = 0. If M13 = 0, a similar cycleing takes place. During block transfer, the time between leading edges of successive Select waveforms is not less than 8.7 microseconds. The P-Register remains set throughout the Instruction. The Block Transfer and Last Word waveforms are in their correct states for the duration of Select and for at least 500 nseconds before and after. Timing diagrams of Block Input, Output and Last Words occur in Figures E, F, G and H.

The following examples demonstrate the shift process.

22.3 Example 1. Left Shift

Assuming an instruction of 0111000000000000110 (F = 14, N = 6) is given to shift the number in the Accumulator and Auxiliary Register six places to the left. Let that number be 0.00000111111000000 (Accumulator) and 1.1111000000111111 (Auxiliary Register), then block 142B is entered to give

Block	Micro-Instructions	Process Counter	O/F Bistables X	Y	R	18 12 5 1
142B	MTF					0000000000000110
	FTG				G	0000000000000110
	GTJ		0	0	J	0000000000000110
	JTPC	6				Set count in PC to 6
144B	QTF					1.1111100000111111
	LTG			1	G	1.1111000001111110
	YTX, GTQ		1		Q	1.1111000001111110
	1TPC	5				PC decremented by 1.
146B	ATF					0.0000111111000000
	XTF					1
	LTG			0	G	0.0000111111000001
	GTA				A	0.0000111111000001
	TPC0	5				Test PC for zero. PC≠0.
144B	QTF					1.1111000001111110
	LTG			1	G	1.1110000011111100
	YTX, GTQ		1		Q	1.1110000011111100
	1TPC	4				PC decremented by 1.
146B	ATF					0.0000111111000001
	XTF					1
	LTG			0	G	0.0001111110000011
	GTA				A	0.0001111110000011
	TPC0	4				Test PC for zero. PC≠0.

Block	Micro-Instructions	Process Counter	O/F Bistables X	Y	R	18 12 5 1
144B	QTF					1.11100000111111100
	LTG			1	G	1.11000000111111000
	YTX, GTQ		1		Q	1.11000000111111000
	1TPC	3				PC decremented by 1
146B	ATF					0.00011111100000011
	XTF					1
	LTG			0	G	0.00111111000000111
	GTA				A	0.00111111000000111
	TPC0	3				Test PC for zero. PC ≠ 0
144B	QTF					1.11000000111111000
	LTG			1	G	1.10000001111110000
	YTX, GTQ		1		Q	1.10000001111110000
	1TPC	2				PC decremented by 1
146B	ATF					0.00111111000000111
	XTF					1
	LTG			0	G	0.01111110000001111
	GTA				A	0.01111110000001111
	TPC0	2				Test PC for zero. PC ≠ 0
144B	QTF					1.10000001111110000
	LTG			1	G	1.00000011111100000
	YTX, GTQ		1		Q	1.00000011111100000
	1TPC	1				PC decremented by 1

Block	Micro-Instructions	Process Counter	O/F Bistables X	Y	R	18 12 5 1
146B	ATF					0.01111110000001111
	XTF					1
	LTG			0	G	0.11111100000011111
	GTA				A	0.11111100000011111
	TPC0	1				Test PC for zero PC ≠ 0.
144B	QTF					1.00000011111100000
	LTG			1	G	0.00000111111100000
	YTX, GTQ		1		Q	0.00000111111000000
	1TPC	0				PC decremented by 1
146B	ATF					0.11111100000011111
	XTF					1
	LTG			0	G	1.11111000000111111
	GTA				A	1.11111000000111111
	TPC0	0				Test PC for Zero. PC≠0

With PC = 0 this indicates the completion of the Function with the number in the Accumulator and Auxiliary Register shifted six places to the left.

22.4 Example 2

When shifting a number to the right, the address is subtracted from 8,192. In the example given below, a total shift of four places to the right is signified by the instruction.
011101111111111100 (F = 14, N = 8188). The result is obtained by reading first the Accumulator and then the Auxiliary Register.

Initially it is assumed that the Accumulator contains

1.1111100000011111 and the Auxiliary Register 0.00000111111000000.

Block	Micro-Instructions	Process Counter	R	18 12 5 1	O/F Bistables Y	X
142A	$\overline{\text{MTF}}$			000000000011		
	1TF			1		
	FTG			000000000100		
	GTJ			000000000100		
	JTPC	4		Set-up P.C. to four		
144A	ATF			1.11111000000111111		
	RTG		G	1.11111100000011111	1	X1=1
	YTX, GTA		A	1.11111100000011111		1
	1TPC	3		PC decremented by 1		
146A	QTF			0.00000111111000000		
	XTF			1		
	RTG		G	1.00000011111100000	0	
	GTQ		Q	1.00000011111100000		
	TPC0	3		Test PC for zero. PC≠0		
144A	ATF			1.11111100000011111		X1=1
	RTG		G	1.11111110000001111	1	
	YTX, GTA		A	1.11111110000001111		1
	1TPC	2		PC decremented by 1. PC≠0		
146A	QTF			1.00000011111100000		
	XTF			1		
	RTG		G	1.10000011111100000	0	
	GTQ		Q	1.10000001111110000		
	TPC0	2		Test PC for zero. PC≠0		

Block	Micro-Instructions	Process Counter	R	18 12 5 1	O/F Bistables Y	X
144A	ATF			1.11111110000001111		X1=1
	RTG		G	1.11111111000000111	1	
	YTX, GTA		A	1.11111111000000111		1
	1TPC	1		PC decremented by 1		
146A	QTF			1.10000001111110000		
	XTF			1		
	RTG		G	1.11000000111111000	0	
	GTQ		Q	1.11000000111111000		
	TPC0	1		Test PC for zero. PC≠0		
144A	ATF			1.11111111000000111		X1=1
	RTG		G	1.11111111100000011	1	
	YTX, GTA		A	1.11111111100000011		1
	1TPC	0		PC decremented by 1		
146A	QTF			1.11000000111111000		
	XTF			1		
	RTG		G	1.11100000011111100		
	GTQ		Q	1.11100000011111100		
	TPC0	0		Test PC for zero. PC=0		

With PC=0 this indicates the completion of the Function with the number in the Accumulator and Auxiliary Register shifted four places to the right.

Note the result is still a negative number due to propagation of the sign digit.

23. FUNCTION 15. INPUT/OUTPUT. PROGRAM TERMINATE

The I-Register will contain 1111, the four bit binary equivalent of the digits 15, or I.1, I.2, I.3, I.4 to give the instruction: If the most significant digit of N is zero, the instruction constitutes an input. If the digit is one, the instruction constitutes an Output or Program Terminate. The instruction is decoded further by the remaining N digits.

Function 15, selected by the F digits allows the N digits of that instruction to reach the P-Register, address and select a specified device in either of the two input or two output channels.

From the control chain, the entrance to Function 15 is at block 150, where the peripheral is selected by MTP and the most significant digit of N is tested by the rise of TM13. The timing diagram Figs. i and j illustrates the action of the relevant waveforms.

The address of the next microprogram is selected by TM13. If M13=0, the conditional CA is generated and the matrix address is that of Block 151A.

The input/Output logic appears on Fig. A13.

23.1 Input Instruction

An Input Instruction is specified when the most significant N digit is 0. Block 151A specify the requirements to select Input channels 1 or 2. In each condition the most significant N digits of the address is 0, and the next most significant N digit is used for input channel selection. The remaining N digits are used for the selection of the required device. For example, an input instruction specifying the tape reader would be set-up as:

B	F	N
0	1111	0100000000000 (15 2048)

With an input from the tape reader 1 P¹n (Input Channel 2) will be selected M13=0, M12=1, Block 152A. The SZ1 waveform sends a select signal to the peripheral with WFP awaiting a reply. When the waveform WFP is true, the timer is arrested. With the reply from the peripheral Z2 becomes false, the timer will again start and continue the operation. This allows the first tape character to be placed into the Accumulator by PTG2 and GTA. This operation is depicted in Fig. A25.

Each tape character comprises 7 digits plus parity, therefore to form one computer word, three tape characters are required. Each tape character is arranged to set the first 7 digit positions of the G-Register, and in order to accommodate successive characters, they are shifted seven places to the left. Therefore each character read must be transferred to the corresponding digit positions of the Accumulator and on reading a second character, is transferred from the Accumulator to the G-Register and left shifted 7 places via wire links. The wire links which left-shift information between the Accumulator and G-Register, are available only on the occurrence of a PTG2 waveform ensuring that the program word being read into the G-Register is built-up in the correct significance. By use of both G and A-Registers for this operation, a full 18 digit word is available as soon as the third character is read. The left shifting operation is arranged so that the first three most significant digits of the first character read are shifted out of range when the third character is placed into the G-Register since they correspond to digit positions of greater significance than the sign. The timing diagram for the Input operation appears in Fig. I.

23.2 Output Instruction and Program Terminate

An Output Instruction or Program Terminate is specified when the most significant N digit M13=1. The F digits of an instruction

select Function 15 in a similar manner to that of the Input Instructions. The micro-instructions in block 151A now test M12 and M11. If M11=M12=1 Block 153A is entered, which is PTR - Program Terminate. If M12=0, or M12=1, M11=0, the block 153B is entered and the select waveform SZ1 sends a select signal to the peripheral and with WFP the computer awaits a reply. The timing diagram Fig. J shows the relationship of the waveforms during an output instruction.

23.3 Select

The select waveform is produced by SZ, which originates in the Control Matrix and the strobe TZ1 which originates in the timer; see Fig. A15. After a delay the reply from the peripheral PR initiates the timing pulse train commencing with t_1 470 nseconds after the incidence of the PR wavefront. The next t4 sets the Select waveform pulse.

23.4 Reply

The Reply waveform signifies to the computer that output information has been accepted by the selected output device or that a specified input device has information available for the computer.

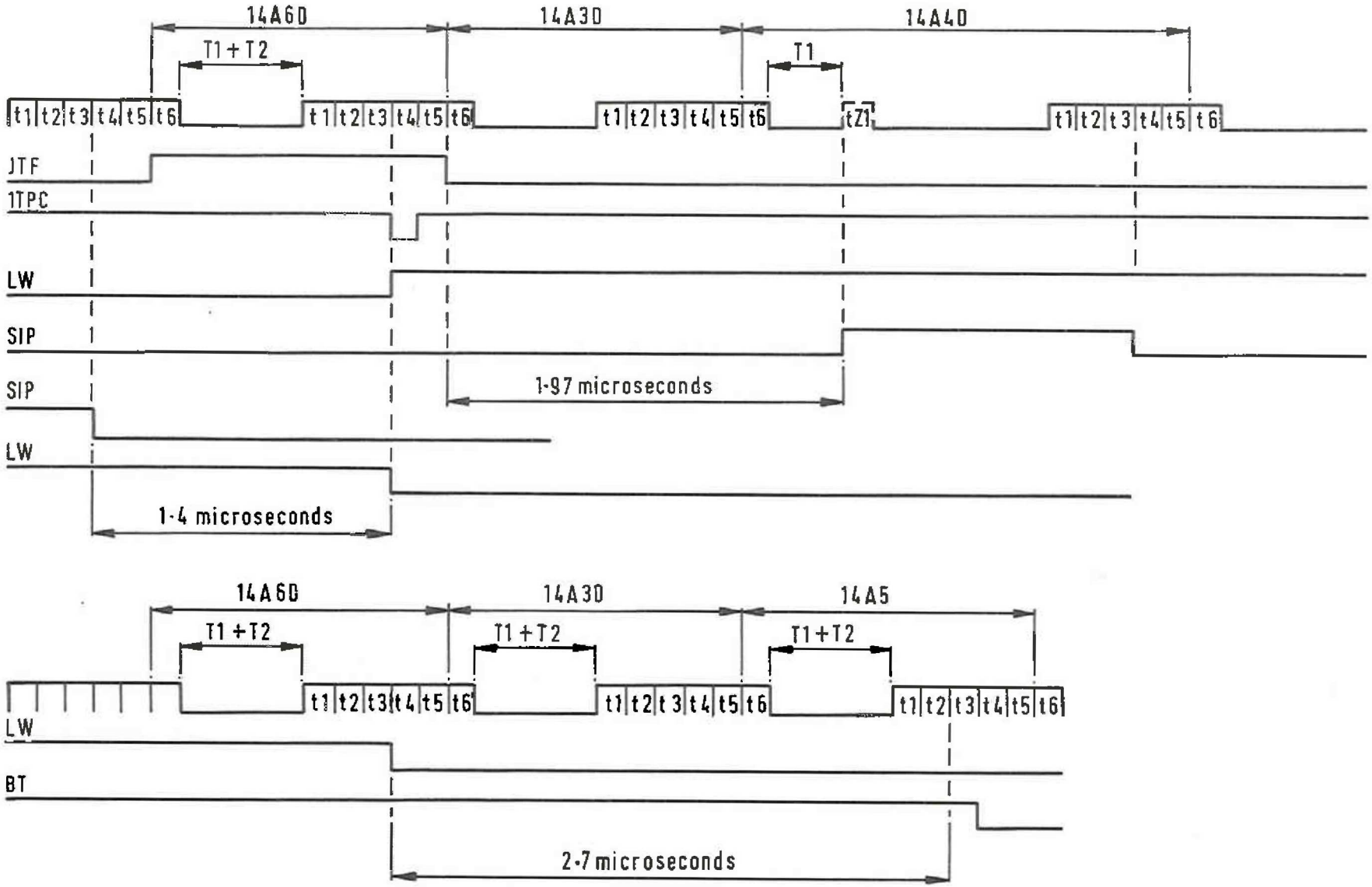
24. STORE CONTROL LOGIC

The circuit of the Store Control Logic is located on the printed circuit board 57A-FM. It operates as a bridge between the waveforms of the Control Logic and the core store. See Fig. K and A13.

24.1 The Functions of the Store Control Logic

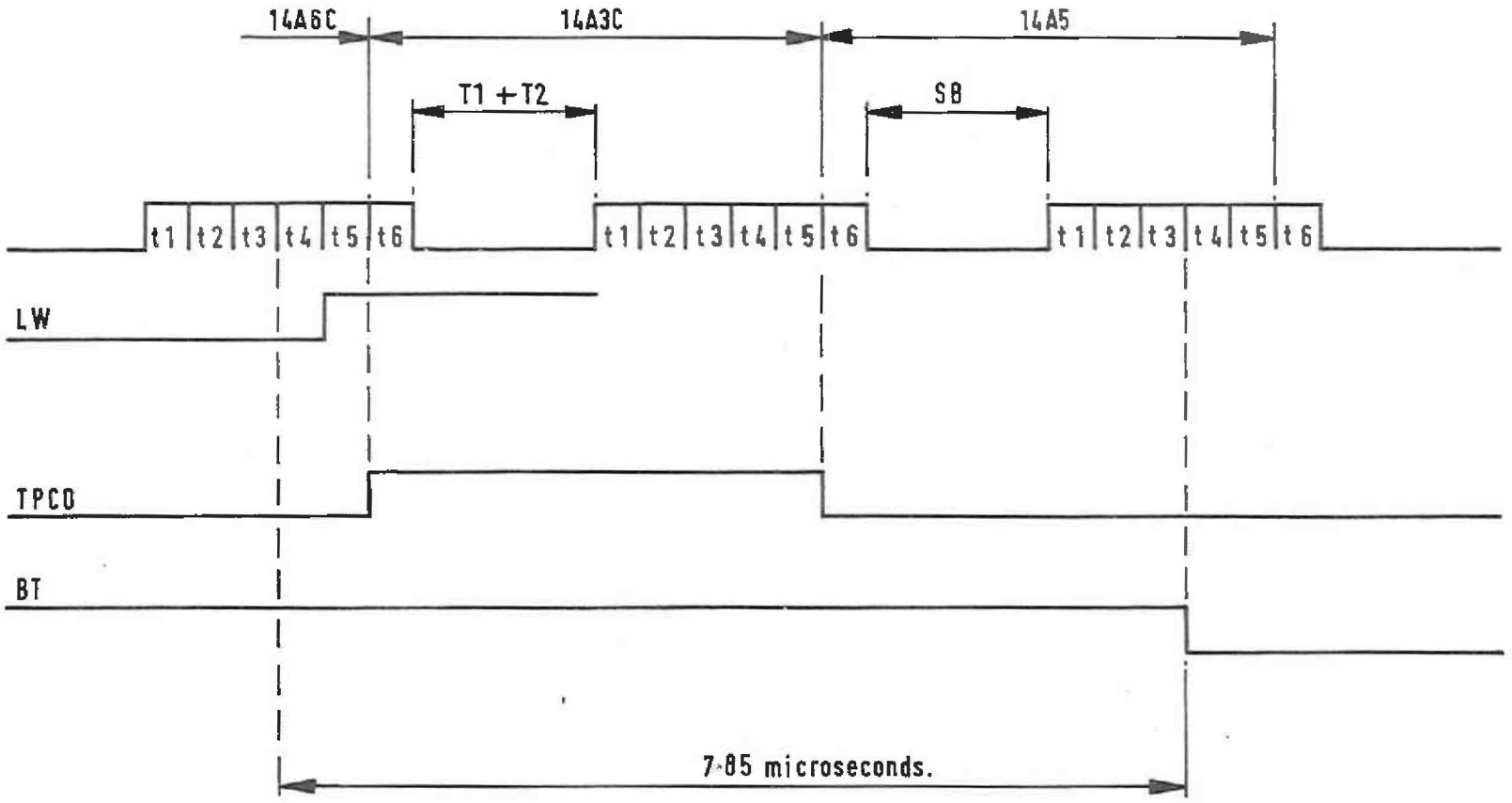
The functions implemented by the Control Logic include:

(i) Conversion of the incident Control Matrix waveforms, Read, Write and Clear into the store operational waveforms $\overline{TR}$, $\overline{TW}$ and $\overline{SSI}$.



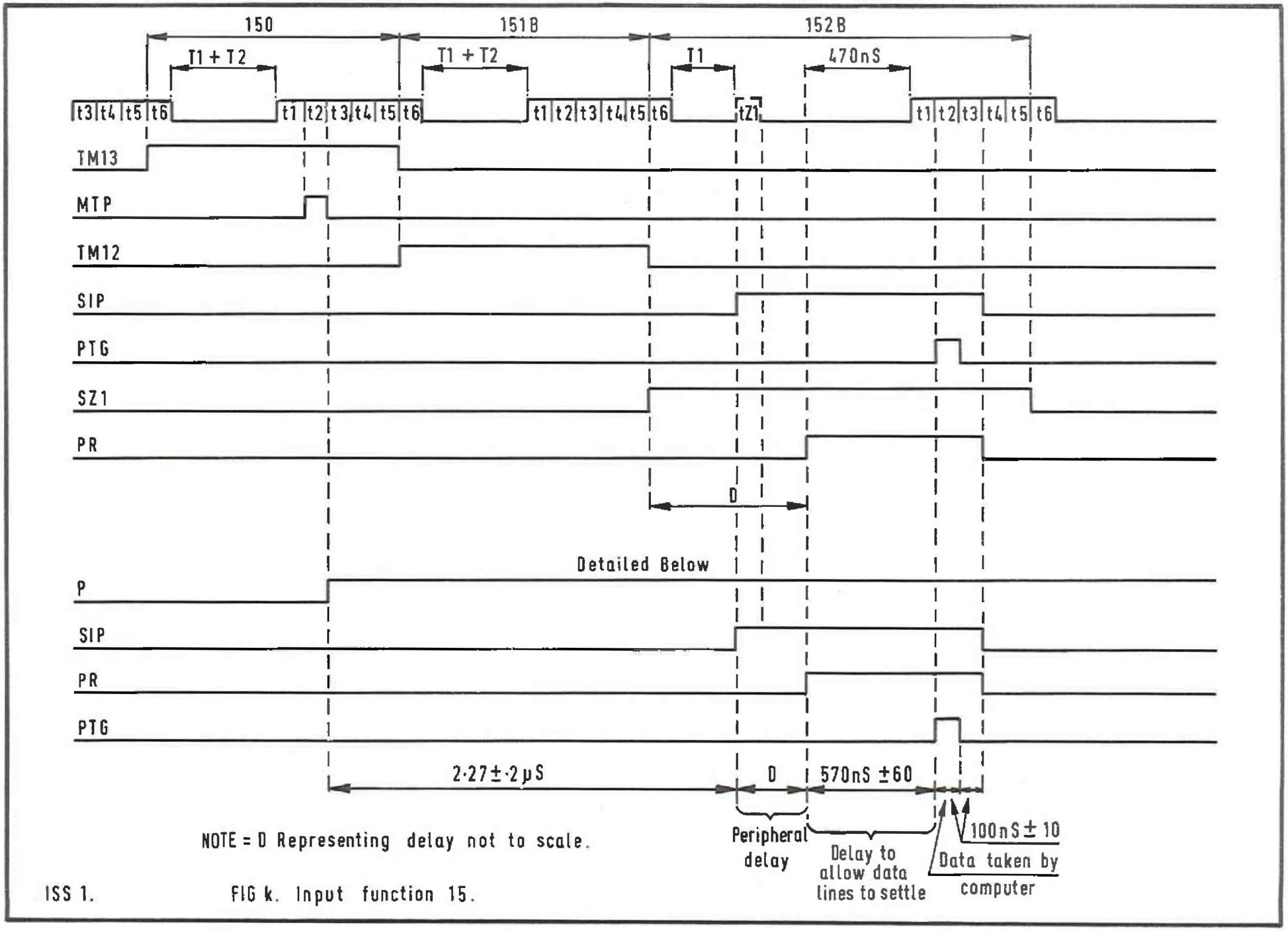
ISS 1.

FIG i. L W Input



ISS 1

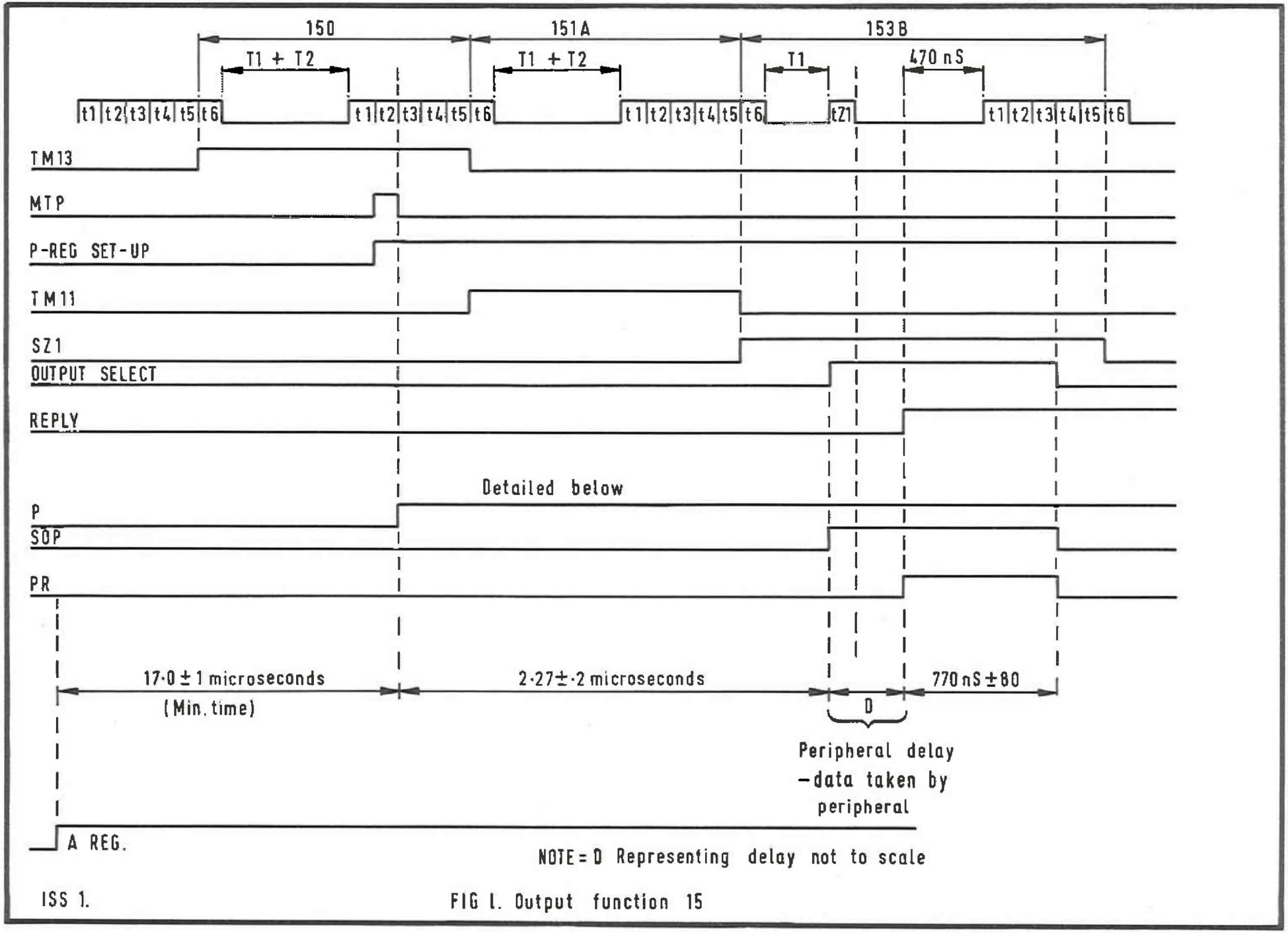
FIG j. L.W. Output.



NOTE = D Representing delay not to scale.

ISS 1.

FIG k. Input function 15.



ISS 1.

FIG 1. Output function 15

(ii) Originates SB, a store busy waveform which sets-up a true condition in the timer arresting its operation for the duration of the 6 microseconds delay necessitated by the Read/Write operation.

(iii) Generates the Initial Instruction waveform IIS.

The waveforms CLEAR, READ, WRITE, $\overline{\text{RESET}}$ and the strobe t5 are incident to the input store control logic gates. These gates are strobed by t5 setting the bistable germane to the operation thus staticizing the demand. The waveforms apropos to the store control logic are detailed in Fig. A18 and in the following:

24.2 $\overline{\text{TR}}$ TRIGGER READ

$\overline{\text{TR}}$ initiates the operation READ from the store. The READ waveform is input to the Store Control and after being strobed by t5 is input to a 330 nsecond monostable. The inverse output of this monostable is $\overline{\text{TR}}$ and the direct output is IIS. (Initial Instruction Strobe). $\overline{\text{TR}}$ also sets a staticizer that ensures that SB is true as soon as $\overline{\text{TR}}$ goes false.

24.3 CLEAR

The implementation of the CLEAR operation is essentially that of READ. The exception being that the waveform which would normally gate the output of the Store Sense Amplifiers into the M-Register bistables is inhibited. This effect is achieved as the CLEAR waveform is strobed by t5. This sets the CLEAR staticizer, thereby setting the $\overline{\text{SSI}}$ waveform false gating the output strobe generator which in turn strobes the sense amplifiers.

The information read into the store is not accepted by the M-Register and hence is destroyed. This leaves the store location Clear for a future WRITE operation.

24.4 $\overline{TW}$ TRIGGER WRITE

The WRITE waveform is strobed by t5 and the output used to set a bistable. When $\overline{TR}$ and $\overline{RGS}$ both become true, the output of this bistable is used to initiate a 330 nsecond pulse. This pulse is TW and after being fed into another inverter comes out as $\overline{TW}$.

24.5 $\overline{RGS}$, $\overline{WGS}$ Delay Logic

The $\overline{TR}$ waveform feeds into the store control chain as diagrammed in Fig. A23, where after a delay of 0.3 microseconds, sets the $\overline{RGS}$ staticizer so that $\overline{RGS}$ is false.

Similarly $\overline{TW}$ sets the $\overline{WGS}$ staticizer so that $\overline{WGS}$ is false but without the 0.3 microseconds delay.

24.6 Store Busy SB. $\overline{SB}$

The SB pulse prevents the reception of additional information during the Read/Write operation, so that SB is up or true for the entire period of 6 microseconds.

SB is true under any of the following conditions:

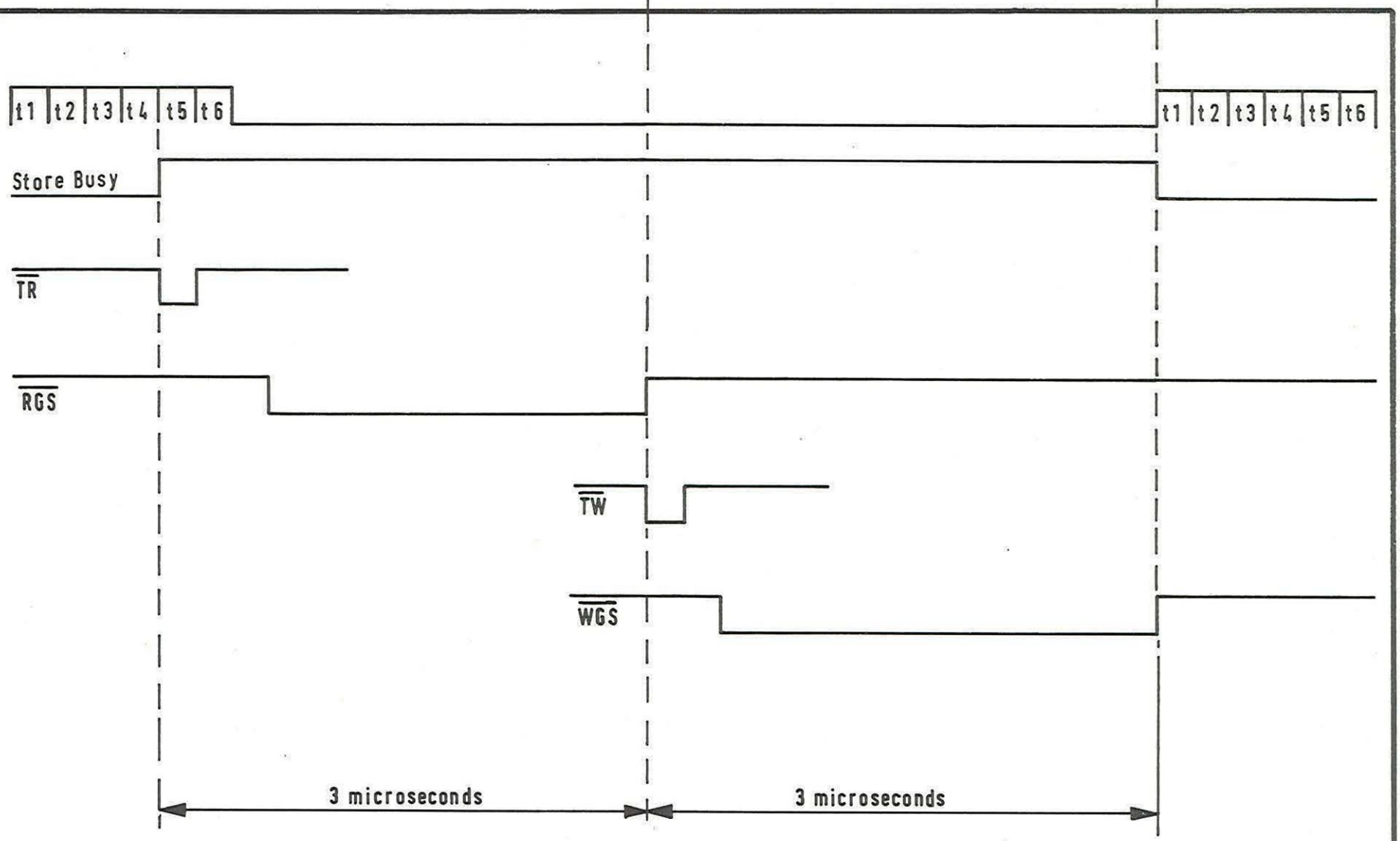
(i) The READ staticizer has been set.

(ii) $\overline{RGS}$ is false.

(iii) The WRITE staticizer has been set.

(iv) $\overline{WGS}$ is false.

While READ and WRITE is being executed SB comes true as soon as $\overline{TR}$ goes false, and SB does not go false again until $\overline{WGS}$ comes true at the end of the cycle.



ISS 1

FIG m. Relationship between SB, $\overline{TR}$, $\overline{TW}$

25. STORE EXTENSION

On the occasions that extra storage facilities are demanded, programs contained in the first 8192 words can access words in the additional storage by the "extended modifier" technique described in Sec. 1.1 and 1-6 in the MCS 920B Computer Specification. It is also possible to use a program in the extra store.

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE No. MCB 143

PART 1: CENTRAL PROCESSOR

CHAPTER 5: THE STORE

CHAPTER 5

THE STORE

CONTENTS

LIST OF FIGURES

THE STORE

1. INTRODUCTION

The memory of the MCS 920B Computer is a random access store comprising 18 planes of 64 x 64 (Y) and 64 x 128 (X) toroidal ferrite cores stacked in a three dimensional matrix configuration functioning as a coincident current magnetic core store with 8192 accessible 18 digit computer word locations. Facilities are available for a store extension to a maximum capacity of 65, 536 words or store locations, the details of which appear in Part 2. The cores in each plane are disposed in rows (designated X-co-ordinates) and columns (designated Y-co-ordinates). The method of stacking and the connections to the stock are illustrated in Fig. n.

The two established remanent states, manifested by the substantially rectangular hysteresis BH curve of a ferrite toroid are uniquely suited to the representation of binary digits 1 and 0. This is depicted in Fig. O.

1.1 Storage and Access of Data

Data is stored or read by two series drive windings (X and Y) that thread all the cores of each plane in lateral and vertical directions. Two additional windings Inhibit and Sense complete the interrogate circuits of the store. Each plane is threaded by an inhibit wire linking all cores of the X-co-ordinate in the same sense. The Sense wire passes diagonally through the cores of one plane linking half the cores in one sense and the remainder in the opposite sense to minimise the cumulative effects of noise. This arrangement is repeated for the 17 remaining planes. The wiring arrangement is repeated for the 17 remaining planes. The wiring arrangement for an 8 x 8 matrix as an example is delineated in Fig. p , where the letters A appearing on the diagram indicate like polarity.

Access to all digits of a computer word simultaneously is obtained by connecting the 18 planes in series by means of the X and Y drive windings. Therefore the incidence of coincident current pulses to a selected pair or X and Y wires will energize the core at the intersection of these wires in each of 18 planes.

Note: Individual sense and inhibit wires are used for each plane. Core drive and selection details and drive at locations in three planes appear in Figs. q and p.

1.2 Read

To read information from a specified core, only the X and Y drives are required, the inhibit drive remains inactive. Two half-current drive pulses are applied to the selected X and Y windings, so that the core at that particular address in each of the 18 planes receives a full pulse of two additive half-pulses.

A core previously switched to the 1 state by the Write operation will be switched to 0 by Read, the resulting change of flux originates a pulse in the Output or Sense windings. Because the sense wire links half the cores in one sense and half in the other, the output may be either positive or negative going.

A core in the 0 state caused by inhibition during the previous write operation will remain unaffected by a subsequent read pulse, and only a small output will be generated.

The selected location is switched into the opposite remanent state after readout, so that information required for future operations must be rewritten into that location while the data remains in the M-register.

1.3 Disturb Pulses

When driven by half currents each core exhibits relatively little output. However the cumulative effect of disturbing large numbers of cores creates a low level random noise. This results from the differing information in the cores and the impossibility of orientating each core so that all fields generated are completely neutralized. The effects of disturb pulses are minimized by the method of threading the sense winding, staggering X and Y Read pulses, properly timing the Read strobe pulse, and using a signal threshold of 15 to 25 mV in the sense amplifiers.

1.4 Write

Information is written into the specified core by the simultaneous application of two coincident current pulses (termed half-currents) of similar polarity and amplitude to the selected X and Y wires. The resultant additive magnetic fields drive the core at the X. Y intersection in the 1 direction. Other cores threaded by the same X and Y wires are only exposed to a field proportional to one half of an X + Y magnetising current, hence because of the substantially rectangular hysteresis BH loop, remain unaffected. See Fig. o.

1.5 Inhibit

The inhibit current is a half current, applied in a direction so as to oppose the X drive write half-current. '0' representation is effected by an inhibit-current flowing through the inhibit wire threading all cores in a particular plane so that all cores of that plane may be inhibited. In each plane when an inhibit current flows whilst the digit position is subjected to X and Y drive the selected core at that position will not be switched, but left in its original '0' state.

2. GENERAL

The method of accessing a particular core is by means of the co-ordinate system. Details of the logic of Selection appear in Fig. A14 and A26.

The X and Y co-ordinate selection is arranged in the following pattern.

XA Co-ordinates	J7 - J12 with J13 selecting one of 64
XB Co-ordinates	J7 - J12 with J13 selecting one of 64
Y Co-ordinate	J1 - J6 selecting one of 64

From the above it may be seen that the utilization of two 64 wire X co-ordinate decode circuits, XA and XB, for an 8,192 word store gives a range of 128 X co-ordinate drive wires.

These circuits are arranged so that each combination of address digits in the J-register results in the selection of one X co-ordinate and Y co-ordinate.

The J-register is decoded by means of the X and Y decode circuits formed by the Read/Write Drivers and Gates of the AED3 boards, in which the Read/Write Gates are strobed to route half current pulses through the X and Y drive wires. In the Read operation, information from the store is strobed by the sense amplifiers and sets the bistables of the M-register.

2.1 Construction

The store of 8,192 words comprises a core store of 18 planes associated with several circuits for access and decode. This is on 21 plug-in units, as depicted in Fig. A3 and set out in Table 1.

TABLE 1

8192 Word Store

Qty.	Unit	Description
1		Core Stack
6	A-AE	Selection Diodes
6	$A\text{-}EA_3$	Sense Amplifiers and Inhibit Drivers
1	$A\text{-}EB_3$	Store Control
1	$A\text{-}EC_3$	Gate Strobe Generator and Master Drivers
5	$A\text{-}ED_3$	Read and Write Gates, Drivers and Decode
1	A-GZ	Temperature Sensing and Control

2.2 Power Supplies

±6V, +15V temperature controlled supply and -16V.

2.3 Power Consumption

Less than 50 watts at $0^{\circ}C$.

2.4 Store Cycling Time

6.0 microseconds nominal.

3. STORE ALLOCATIONS

The locations 0-7 of the store are reserved for the Sequence Control Register and Modifier Register for the various program priority levels. Reference to these locations are legitimate if their limits are given consideration. The contents of these locations may be over-written by the program as shown by the following example:

10	1	Increment B-register (level 1)
5	6	Jump to location specified by A (level 4 operative) or set level 4 starting address to the contents of A (level 4 not operative).

The locations 8180 to 8191 inclusive are not available for storage. They are reserved for initial instructions under which the control program loading is implemented. These locations may be read as either fixed instructions or numbers, but cannot be overwritten or changed in any manner by the program. Refer to Pt. 1, Chap. 1, Sec. 3.4.

3.1 Sequence Control Register (SCR)

The contents of the four Sequence Control Registers (SCR) are in locations 0, 2, 4 and 6. The SCR's hold the address of the next instruction to be obeyed for each of the four program levels. The SCR is incremented by one address each time an instruction is obeyed, or replaced by a new address in a Jump instruction.

3.2 The B-Register

Locations 1, 3, 5 and 7 hold the B-register for each program level. Each location holds an instruction modification or count instruction relevant to one of the four program levels and is selected when the sign digit of an instruction is a 1.

B-modification is a means of modifying the N-digits of an instruction by the addition of the B-register content to the address before the instruction is obeyed. The Function F digits or stored instructions are unaffected.

The store locations associated with the four program levels appear on the next page in order of priority.

Program No.	B-Register Location	SCR Locations
1	1	0
2	3	2
3	5	4
4	7	6

4. THE DRIVE SYSTEM

4.1 Address Decode and Selection Circuits

The drive system of the store is assembled on five A-ED3 and six A-AE printed circuit boards. Each A-ED_3 board comprises eight driver and eight gate circuits. The A-AE boards hold the isolating diodes for the selection system.

The logic of the drive system and the decoding arrangement are shown in Figs. A14 and A15, being similar in all pertinent circuits. The configuration of the Drivers and Gates necessary to route a read or write half-current through one of the 64 drive wires of a co-ordinate may be determined by inspection of the relevant drawing.

The X co-ordinate selection system is effectively doubled to yield the necessary 128 drive wires. The numbered positions 1-64 denote the X or Y co-ordinate drive wires, the symbols at these points being graphical representations of co-ordinates that pass through the ferrite cores of the 18 planes. See Fig. A26 for the Y selection system and Figs. A27 and A28 for the X1-64 selection systems.

Decode of the J-register is effected by either Read or Write Drivers for both Read and Write operations. A Read Driver selects a Write Gate, conversely a Write Driver selects a Read Gate. Address information is arranged so that digits J1 - J6 select Y co-ordinate Read

and Write Drivers. Digits J7 - J13 select X co-ordinate Read and Write Drivers.

The selection of a particular Y-drive co-ordinate is detailed in Section 4.2, Read Cycle.

If a read operation is to be executed, bits 1-6 of the J-register will select both a Y Read Driver and Write Driver as shown by Fig. A26. The specified Read Drivers will then select eight Y-drive wires (either 1, 2, 3, 4, 5, 6, 7 and 8 or 9, 10, 11, 12, 13, 14, 15 and 16 etc., thereby effecting the first level of decode by reducing the number of possible Y-drive conductors to eight. The Write Driver selected at the same time as the Read Driver executes a second level of decode for the Y co-ordinate by selecting an additional eight Y-drive conductors in a matrix configuration. This will therefore be in the range of either 1, 9, 17, 25, 33, 41, 49 and 57, or 2, 10, 18, 26, 34, 42, 50 and 58 etc.

The selection of the X co-ordinates is an identical procedure, the drivers and gate selected being determined by address digits in the range J7 to J13 or $\overline{J13}$.

The decode of J1 ⟶ J6 will select one Y co-ordinate. The decode of J7 ⟶ J13 will select one X co-ordinate, resulting in the store location at the selected X/Y intersection being driven by the additive half-currents of the X and Y Read and Write Drivers.

4.2 The Read Cycle

The entire selection system is of symmetrical format with directly coupled logic circuits

Fig. A30 is a simplified operational diagram of the Y-selection system based on the Y-selection drawing, Fig. A26 and General Flow Diagram.

Fig. A14 illustrates the selection of a particular Y co-ordinate.

The corresponding drive and gate circuits as shown in Fig. A26 are connected so that when a driver is selected, the corresponding gate will also be selected if its gating waveform is true. The gating waveforms are known as Read Gate Strobe and Write Gate Strobe. They are true for the whole period of their respective cycles and with the address bits, together select the appropriate gates.

When selected both gates and driver are at low impedance and set the path for the drive current which is controlled in magnitude and timing by the master driver.

The Read and Write Gate Strobe waveforms are generated by the store timing board ($58/A\text{-}EB_3$) and buffered by drivers on the Master Driver board ($59/A\text{-}EC_3$). The waveforms of the Read Cycle appear in Fig. s.

The necessary control waveforms for the Read Cycle are derived from a chain of monostables on the $A\text{-}EB_3$ board (Fig. A23) and triggered by $\overline{TR}$ which is output from the store control board A-FM.

The $A\text{-}EB_3$ board provides the following waveforms for the Read Cycle:

$\overline{RGS}$	selects the appropriate gates and drives the steering circuit.
$\overline{RX}$ and $\overline{RY}$	switch on the X and Y Master Drivers.
$\overline{STROBE}$	gates the '1' output from the sense amplifier.

Immediately after the receipt of $\overline{TR}$, $\overline{RGS}$ implements two actions:

(i) The gates of the selection system are selected.

(ii) The path of the Read drive current is selected.

See Fig. A33.

The first is achieved by using $\overline{RGS}$ to switch on VT9 and VT10. Secondly, VT28 and VT31 are switched to a low impedance and VT27 and VT32 to a high impedance by the $\overline{RGS}$ waveform input to VT7.

Approximately 0.5 microseconds after the receipt of $\overline{TR}$, $\overline{RY}$ switches-on the master driver to allow current to flow along the previously selected route. The rate of current rise is controlled by the feedback amplifier comprising VT20, VT22, VT23, VT24 and VT25. The current will rise until the voltage across the 5 ohm resistor R58 equals the input of the temperature controlled reference voltage. This is 1.3 to 1.4 volts.

$\overline{RX}$ switches on the X-master drivers but with a delay of approximately 0.1 microseconds after $\overline{RY}$.

$\overline{STROBE}$ from the store timing board switches-on VT13 of the output strobe generator on the A-EC3 board approximately 1.6 microseconds after the receipt of $\overline{TR}$. The output of the Output Strobe Generator is input to the 18 sense amplifiers. The leading edge of the STROBE pulse in the sense amplifier should coincide with the peak output of a core which had previously been storing a '1'.

Approximately 2.4 microseconds after the commencement of the Read Cycle, the Read X and Y currents are switched-off. At 2.7 microseconds RGS is switched off and the store is ready to start the Write Cycle.

4.3 Write Cycle

If a word is to be written into a specified store location, a procedure similar to the read operation is implemented. The X and Y drive wires write '1's into the 18 digit positions of the store location selected by the N digits unless prevented by an inhibit current.

During the Write cycle, the contents of the M-register determine the digit positions to be inhibited. Thus, where a digit position is required to represent a zero, an output current from the inhibit driver associated with that plane is initiated. This current flows in opposition to the X co-ordinate Write current thereby nullifying the X-drive. With a Y half-current only, insufficient flux is generated to affect the inhibited ferrite core. Waveforms pertinent to the Write cycle appear in Fig. t.

The Write and Read cycle controls being similar, the necessary control waveforms are derived in like manner. The Write cycle waveforms are triggered from the 58/A-EB 3 board by $\overline{\overline{TW}}$ which outputs the waveforms $\overline{\overline{IP}}$, $\overline{\overline{W}}$ and $\overline{\overline{WGS}}$ to select the pertinent gates, and driving the steering circuit as seen in Figs. A23 and A33, but with the following differences:

(i) The direction of current flow through the drive wires, is in opposite sense to that of Read.

(ii) The WGS pulse switches VT4 of the Write Gate B through VT3 into a condition of low impedance.

$\overline{\overline{RGS}}$ not being active (+ve) VT7 is switched off and VT8 is switched on. This switches VT27 and VT32 to low impedance and routes the write current through the selected gate and driver. The amplitude and timing of the write currents is controlled by the X and Y master drivers which derive their input from $\overline{\overline{W}}$ on the 58/A-EB3 board, Fig. A23.

4.4 Driver and Gate Circuit

The Driver and Gate circuit is selected when the appropriate address bits are applied to a four input NAND gate (D1 to D4 and VT1 given by Fig. A29). The output of this gate (clamped to 0V by D5 and D6) provides bias to both Driver circuit (VT2) and Gate circuit (VT3).

Note: Where VT2 is a Read Driver, VT3 is the Write Gate (or Read Gate where a Write Driver is selected, Fig. A30 refers). When the associated Master Driver is switched-on, VT2 presents a low impedance in the driver path.

To prevent possible oscillation, a 68 pF capacitor is connected between base and collector of VT2.

4.5 Gate Circuit

The Gate circuit consists of VT3, VT4, diodes D7 and D8 together with R5. When a gate is selected, the base of VT3 is taken positive relative to its emitter and switches on. This switches on VT4 to allow a low impedance for drive current.

5. SELECTION DIODES (72-77/A-AE UNIT)

The function of the selection diodes is to control and direct the flow of drive current through the windings of the specified cores and prevent circulating currents flowing through the core stack. For each co-ordinate of the X and Y selected system, four selection diodes are required; there are 128 diodes to each A-AE circuit board. Six A-AE boards are required for 8,192 word stores.

Disposition of the diodes is depicted on the Selection System drawings A26, A27 and A28 and on the Selection Diode boards, Fig. A32.

6. MASTER DRIVERS (59/A-EC3 UNIT)

The electrical circuits on the 59/A-EC3 unit implement several functions. These circuits appear on Fig. A33 and are as follows:

(i) Power Supply Correct (PSC) Receiver and Delay
(ii) Inhibit Buffer
(iii) Steering Circuit
(iv) Master Drivers
(v) Gate Strobe Generator
(vi) Output Strobe Generator
(vii) Temperature Controlled Voltage Reference

6.1 Power Supply Correct (PSC) Receiver and Delay

The signal from the power unit is used in the computer to enable it to be stopped, if computing, before the power lines decay and to prevent the machine starting before the power lines are correct.

The $\overline{\text{PSC}}$ waveform is input to the center of a voltage divider across the +15V variable and 0V supply. When the voltage is correct the input to VT1 is at 0V. VT1 is switched off and the waveform PSC at pin 27 is up. In this state the Inhibit Buffer operates normally. If the input $\overline{\text{PSC}}$ goes positive, a voltage will appear at the base of VT1, switching it to a low impedance. This will stop the machine at the end of its current cycle. The waveform of PSC (pin 27) will fall, VT2 will be switched-off for approximately 15 microseconds. VT2 being switched-off maintains VT3 switched-on and holds VT4 switched-off. After approximately 15 microseconds VT2 switches-on, VT3 switches-off and VT4 switches on clamping the output of the Inhibit Buffer to 0V. The computer switches off retaining the contents of the store, but loses the contents of the registers.

6.2 Inhibit Buffer

The Inhibit Buffer isolates and provides the power to drive the 18 inhibit drivers on the A-EA3 board. The input to the buffer is from the IP bistable on the A-EB3 Store Control Unit. The IP bistable is set and reset by the chain of monostables on the A-EB3 Unit.

The circuit comprises two transistors, VT5 and VT6, connected as shown in Fig. A33. Input to the Inhibit Buffer is $\overline{IP}$, the output is IP.

6.3 Steering Circuit

The function of the Steering Circuit is to control the direction of current flow in the Master Drivers during a Read or Write operation.

The circuit of the Steering Circuit includes the diodes D11, D12 and D13, the transistor VT7, VT8 and their associated resistors.

The input waveform $\overline{RGS}$ actuates the Steering Circuit to supply base current for the selected super-alpha pair of the master drivers. The flow of current through the super-alpha pairs is initiated by $\overline{RX}$, $\overline{RY}$ during the Read cycle and by $\overline{W}$ during the Write cycle. The magnitude of this current is determined by the Reference Voltage from the Temperature Sensing board 65/A-GZ.

During the operation of a Read cycle when $\overline{RGS}$ is at 0V, the collector of VT7 will rise to zero volts as the collector of VT8 falls to -6V. Base current for the two super-alpha pairs of the master drivers (VT28-29 for Y and VT30-31 for X) which initiate the Read currents is then available through VT7.

During the Write cycle when $\overline{RGS}$ is at +6V the collector voltage of VT7 will fall to -6V, while that of VT8 rises to zero volts.

This selects the two super-alpha pairs of the master drivers (VT26-27 for Y and VT32-33 for X) and routes the drive current through the Write drivers and gates.

6.4 The Master Drivers

The function of the Master Drivers is to supply a timed drive pulse to the X and Y decode and selection circuits (drivers and gates) in response to input pulses from the Store Control Chain unit A-EB3 board.

The inputs are:

(i) Read X $\overline{RX}$
(ii) Read Y $\overline{RY}$
(iii) Write $\overline{W}$

When the write waveform $\overline{W}$ occurs, it is common to the inputs of both X and Y Master Drivers.

In the drawing Fig. A33 the outputs of the Master Driver super-alpha pairs are IWY, IRY, IRX and IWX.

The Master Drivers are arranged into two separate circuits to provide X and Y drive currents. The same circuit is utilized for both read and write Master Drivers. The actual routing of the current is controlled by the Steering Circuit which drives the super-alpha pairs.

After the selection of the pertinent super-alpha pairs of the Master Drivers by the Steering Circuit, the actual implementation of the drive currents occur in the following manner.

When the waveform $\overline{RX}$ goes true or becomes 0 volts, VT38 is turned on, which in turn switches on the super-alpha pair VT36-37. Current flow is thereby established from the variable supply through the Read Input gates and Read drivers of the core selection system through VT30-31, VT36-37 and R69, to -6V.

The magnitude of the current flow is determined by the voltage drop across R69 (high stability). This voltage is compared by the comparator amplifier VT39 with a reference voltage which has been derived from the temperature sensing board. When the voltage across R69 equals the reference voltage the current drive to VT37 is limited. This reference voltage may be adjusted to give the correct drive current. This is normally in the range 1.35V to 1.4V at room temperature.

The voltage across R69 may be varied when margins are applied by the use of a potential divider arrangement which artificially increases or decreases the voltage appearing at the junction of R41-R42.

Although the foregoing sequence is initiated by the waveform $\overline{RX}$, the waveforms $\overline{W}$ and $\overline{RY}$ also operate in the same manner.

The waveshape of the forward and trailing edges of the drive current is determined by the feedback circuit comprised mainly of VT34-35 and C9-R72 and R73 to give the correct trapezoidal waveshape at time of manufacture.

6.5 Gate Strobe Generator

The function of the Gate Strobe Generator is to originate waveforms controlling core selection in the store. The input waveform $\overline{RGS}$ generates RGS_1 and RGS_2 through VT9 and VT10. $\overline{WGS}$ generates WGS_1 and WGS_2 through VT11 and VT12.

RGS_1 and RGS_2 are distributed to the Read Gates of the store selection circuits. WGS_1 and WGS_2 are similarly routed to the Write Gates of the selection circuits.

The sequence of operation is shown by Fig. A33.

6.6 Output Strobe Generator

The function of the Output Strobe Generator is to supply a STROBE waveform to the sense amplifiers. The circuit comprises VT13 and VT14 together with the associated gating diodes. The three input waveforms are:

(i) $\overline{\text{STROBE}}$ Strobe

(ii) $\overline{\text{IIG}}$ Inhibit Initial Instruction

(iii) $\overline{\text{SSI}}$ Store Strobe Inhibit

6.6.1 $\overline{\text{STROBE}}$

This waveform is negative going and is generated by the 58/A-EB3 board (Store Control Chain) during the Read Cycle. If it occurs when $\overline{\text{IIG}}$ or $\overline{\text{SSI}}$ is at +6V, a strobing pulse will appear at the STROBE output and is distributed to the sense amplifiers.

6.6.2 $\overline{\text{IIG}}$

If the Initial Instructions are being used from locations 8181 to 8191, $\overline{\text{IIG}}$ will be at 0V and will prevent the input $\overline{\text{STROBE}}$ from switching on VT13 and producing an output pulse.

6.6.3 $\overline{\text{SSI}}$

$\overline{\text{SSI}}$ inhibits strobe during the read cycle so that information read out of store is lost. The location is cleared preparatory to writing new information. If $\overline{\text{SSI}}$ is at 0V then VT13 cannot be switched on by $\overline{\text{STROBE}}$. $\overline{\text{SSI}}$ originates from a staticizer on the store control board (A-FM). The staticizer is set by the matrix waveform clear.

6.7 Temperature Controlled Voltage Reference

The Voltage Reference from the temperature sensing board A-GZ is input to VT15 and a proportion of it appears across RV1. VT16 and VT17 form a differential amplifier with feedback via VT19. The feedback action of VT17 and VT19 is such that the output voltage from the emitter of VT19 to -6V is always equal to the input voltage applied to the base of VT16. The output voltage is distributed to the bases of VT20 and VT39 to control the magnitude of the Read and Write currents.

7. INHIBIT DRIVERS (65-71/A - EA3 UNITS)

The function of the Inhibit Drivers is to apply a drive current to inhibit wires of one or more store plane during the Write Cycle so that "0" representation is obtained, see Fig. A24.

The word to be written into a specified store location is contained in the M-Register. Digit positions holding a "0" will have a '1' (+6 volts) appearing at the $\overline{M}$ output. It is the $\overline{M}$ outputs which provide the input signals to the inhibit drivers in the corresponding digit positions.

Three inhibit drivers are provided on each of six printed circuit boards for a total of 18 inhibit drivers, one driver to each bit of the 64 x 128 matrix plane. These circuit boards are shared with the 18 sense amplifiers similarly arranged. The inhibit drivers route a half-current through the inhibit windings located in the X axis. The direction of inhibit current flow is such that it is in opposition to the Write X drive half current and prevents development of the full core switching current.

To prevent the possibility of cores being switched in positions where a zero is to be stored, the inhibit currents generated by the inhibit drivers must be at their maximum value (determined by the temperature

controlled power supply) before write currents are applied. This is accomplished by generating inhibit drive before the leading edge of th write pulse as shown in Fig. A23. The timing of the inhibit drive is controlled by the waveform IP which originates from the Store Control Chain (A-EB3 Unit).

7.1 The Circuit

The schematic diagram of the inhibit drivers is depicted on Fig. A24 and the circuit operation is as follows:-

The input of the +6V IP waveform and +6V $\overline{M}$ waveform of the AND gate diodes D10 and D11 switches on VT11, thus providing base current for VT12 via D13 and switching it on. The diode D12 prevents saturation of VT12. The network C10, R24 and R25 improves the rise time of the current and controls its amplitude. The resistor R27 connected across the inhibit winding is used as a damper when the current is removed. C12 decouples the inhibit power supply.

8. SENSE AMPLIFIERS (65-71/A-EA3 UNITS)

The input to the sense amplifiers is taken from the sense winding of the store. These pulses are of ill-defined shape and amplitude. The resultant output pulse is of accurately timed standard amplitude (+6V to 0V negative going). The circuit of the sense amplifiers may be seen in Fig. A24.

The following waveshapes are input to the sense amplifiers. The matrix sense windings pick up four types of waveshapes which are input to the sense amplifier.

(i) The correct Read 1 pulse as the core switches.

(ii) A disturbance when the remaining cores do not switch.

(iii) A correct size pulse occurring at a time when no Read pulse is required (Write 1).

(iv) A large pulse due to Inhibit Current (Write 0).

8.1 The Circuit

Three sense amplifiers and three inhibit drivers share a single A-EA3 board. The sense amplifier is essentially a discriminator circuit rejecting conditions (ii), (iii) and (iv) but accepting condition (i).

The sense windings are connected to the bases of the dual transistor VT1 which forms a longtailed pair. RV1 is provided to equalise emitter currents so that zero potential exists between the collectors of VT2 and VT3.

The collectors of VT1, respond to inputs of either polarity arriving at the bases. The collectors are directly connected to the bases of the pair VT2 and VT3.

Diodes D1 and D2 prevent the circuit being overloaded with large signals. Thermistor S1 adjusts the circuit to temperature changes. R3 adjusts the threshold by controlling the potential at the emitter of VT4 and VT5.

VT4 and VT5 share a common emitter load, and the output across the load will always follow the more positive of the inputs to the bases of VT4 and VT5. The amplifier is biased so that the voltage at the common emitter point of VT4 and VT5 without input is approximately -1.5V. The output from the sense winding is 50 mV approximately. This is amplified to appear at the common emitter point of VT4 and VT5 as 2.6V.

In the absence of STROBE VT6 cannot switch on as there is no base current available (D3 may be back biased). When STROBE goes to +6V, VT6 will switch-on giving a '1' output if the potential of the common emitter point of VT4 and VT5 is sufficiently positive. This is when the potential is greater than 0V, and corresponds to a positive signal of the emitters of VT4 and VT5 at greater than 1.5V.

In checking the operation of the store, this is a convenient monitoring point. (See Fig. s, Typical '1' output).

9. STORE CONTROL CHAIN (58/A - EB3 UNIT)

The Store Control Chain comprises the networks (Read and Write Cycle Control) mounted on a single type A-EB3 printed circuit board.

The unit is designed to implement the Read and Write Cycle control of the store circuits by generating the waveforms that govern the Read and Write cycle operations. The waveforms $\overline{RGS}$, $\overline{RY}$, $\overline{RX}$, $\overline{STROBE}$ $\overline{IP}$, $\overline{W}$, $\overline{WGS}$ are originated by the unit when triggered by $\overline{TR}$ or $\overline{TW}$ which originate from the Store Control board (A-FM).

The timings ensure that the pulses maintain the correct timing relationship to each other to achieve optimum drive conditions to the core store.

The timing, pulse duration and pulse relationships of the Read and Write Cycle Control appear on Fig. A23

9,1 Read Cycle Control

The Read Cycle Control is an assembly of eight monostable elements of differing time periods, four NAND gates arranged as a pair of bistables and a single diode input NAND gate.

The Read Cycle Control functions as a controlled delay in which the co-ordinates of the store drive circuits together with strobing is effected, the operating being initiated by a Trigger Read (TR) pulse produced in response to the microprogram.

The output of VT4-1 is a positive going pulse input to the monostable R1 to trigger it with the positive going edge. The output of VT4-1 is inhibited if $\overline{SIS}$ (Suppress Internal Store) is at 0 volts. A diagram of the Store Control Chain may be seen in Fig. A23.

9.2 Read Cycle Control Circuit

Monostable R1 (0.3 μs) and R2 (0.2 μs) are triggered in succession by the input trigger $\overline{TR}$ which has been inverted by VT4 (1).

This sets the staticizer formed by VT4 (2 and 3) to give an output $\overline{RGS}$. The setting delay is equal to the duration of monostable R1.

The staticizer formed by VT4 (4 and 5) is set after a delay caused by monostable R2 to give an output $\overline{RY}$, $\overline{RX}$ output is delayed by monostable R3 and its duration determined by monostable R4. The positive going edge of monostable R4 output triggers monostable R5, resetting staticizer VT4 (4 and 5) and its output $\overline{RY}$.

The positive-going edge of monostable R5 triggers monostable R8 which resets $\overline{RGS}$. The timing of $\overline{Strobe}$ relative to the leading edge of the read current is determined by monostable R6 and the strobe duration set by monostable R7.

The two staticizers are also reset when the logic is in the reset state.

9.3 Write Cycle Control

The Write Cycle Control is very similar to the read cycle control having a number of monostable and staticizer circuits. A block diagram with a timing diagram of the Write Cycle Control chain appears on Fig. A23.

The Write Cycle Control chain provides the timing waveforms for the generation of write current and inhibit current pulses of the correct duration and timing relative to each other.

The Write Cycle Control chain provides three output waveforms:-

(i) $\overline{\overline{WGS}}$

(ii) $\overline{\overline{IP}}$

(iii) $\overline{W}$

The monostables W1-W4 control the setting of two staticizers for $\overline{\overline{IP}}$ and $\overline{\overline{WGS}}$ and provide the waveform $\overline{W}$ in exactly similar manner as in the read control chain.

9.4 Operation of the Monostable Circuit

The circuit is triggered by a positive going pulse to C1. The input is differentiated by the network C1-R1 and applied to the base of VT1 resulting in a negative pulse to the cathode of D1. The negative pulse is applied to VT3 switching it off and switching on VT2. The cathode of D1 now remains at 0V even though VT1 is no longer switched on while the capacitor on the base of VT3 charges up positively through R4.

When the base potential has risen to approximately 0.5V, VT3 switches on again switching off VT2 so that the output rises to +6V.

The two monostable circuits are identical in operation, only resistor R7 has been added in some positions to improve noise immunity on the output.

10. TIMING CONSIDERATIONS

10.1 Cycle Time

The cycle time is directly related to core, decode circuit and amplifier recovery times. These are the prime influences on the speed of operation. The time a core takes to switch is dependent upon its composition and physical size. This switching time is approximately 1.3 microseconds and allowing for decode selection and current rise times etc., gives a read or write cycle of 2.8 microseconds. If a write cycle immediately follows a read cycle, the read-write cycle takes 5.6 to 5.8 microseconds.

10.2 Drive Current Pulses

The X and Y drive current pulses must overlap for a minimum period during the read or write cycle which is at least equal to the switching time of the cores (1.3 microseconds). To achieve this with the circuits used, the currents are set so that their peak amplitudes occur for a longer duration than 1.1 microseconds.

10.3 Inhibit Current

Where zeros are to be stored, it is unnecessary to switch the selected core, the inhibit currents generated by the inhibit drivers must be at their maximum value of approximately 220 mA before write currents can switch the core. To accomplish this the inhibit drivers are turned on by the inhibit waveform IP and the appropriate $\overline{M}$ digit before the waveform $\overline{W}$ turns on the write Master Driver.

10.4 Strobe

The width of the strobe pulse is 0.3 microseconds. It is timed so that the leading edge coincides with the peak value of the amlified core output.

10.5 Read and Write Gate Strobes

The minimum time that the Read and Write gates are open is the period during which drive currents are being generated. In practice the Read and Write gate strobe signals are made rather longer as they control the store busy signal on the A-FM (Store Control) board and hence the speed of operation.

11. TEMPERATURE SENSING AND CONTROL (65/A-GZ UNIT)

The function of the Temperature Sensing circuit is to sense the temperature in the ferrite core stack by means of nine series connected diodes mounted within it. A reference voltage is produced which is a function of the core stack temperature; this is used to change the store drive currents and provide, by means of comparator circuits, logic signals when the core stack is operated outside the normal temperature range. A block diagram depicting the functions of the A-GZ unit is given in Fig. A34 and the circuit in A35.

11.1 The Circuit

As seen from Fig. A34, the circuit can be considered to be several circuit elements:

(i) Voltage Reference Generator

(ii) Temperature Sensing Circuits

(iii) SCR Bistable and Control Logic

(iv) Store Heater Power Amplifiers

11.2 Voltage Reference Generator

The circuit is depicted in Fig. A35 and comprises VT1, VT2, VT3, VT4, DI and associated resistors. VT1, together with D1, R1, R2 and R3 comprise a constant current generator providing a current of 2.5 ±0.1 mA to the forward biased diodes within the core stack. R3 is selected to adjust the current when the unit is tested. The voltage across the diodes is +5.7 ± 0.3V at +20°C and changes at -0.3% per °C temperature rise. VT2, VT3, VT4 and R4-R10 form the reference voltage generator. VT2 and VT3 form a comparator circuit with VT4 as the series regulator. The output from the emitter of VT4 is set to +8.65V at 20°C by selection of R8 during manufacture. If the core stack or stack diodes are changed in the field the reference voltage should be checked and R8 reselected. It should be noted that R9 is not taken to 0V but to approximately +3.7V (junction of R60 and R61). This modifies the output voltage change to -0.42% per °C which optimises the core stack currents with respect to temperature.

11.3 Temperature Sensing Circuits

There are three temperature sensing circuits on the A-GZ board.

(i) Over temperature sensing circuit

(ii) Under temperature sensing circuit

(iii) Store heaters off and restart circuit

11.3.1 Over Temperature Sensing Circuit

VT5, VT6, VT7, VT8 and the associated circuit elements comprise the over temperature sensing circuit functioning to switch off the computer in the event of excessively high temperatures arising in the core stack.

The over temperature circuit is adjusted to trip if the reference voltage falls to +7.2V so that if this potential appears at the VT5 - VT6 comparators, VT5 will switch-off and VT6 will switch-on. VT6 switching on will in turn switch-on VT7 and VT8 sending out the logic signal $\overline{\text{OVERTEMP}}$. This may be used by a power supply unit such as MCB 21 to switch-off the computer power.

11.3.2 Under Temperature Sensing Circuit

The transistors VT12, VT13, VT14 and their associated resistors and capacitor comprise the under temperature sensing circuit.

Resistors R26 to 29 are adjusted during manufacture so that a reference voltage of +9.9V will actuate the VT12-VT13 comparator. VT12 switching on will in turn switch on VT14 and trigger the SCR bistable VT22. VT22 switching on switches off VT20, and VT23 in turn is switched on. The logic signal STC (Store Temperature Correct) goes down and stops the computer. This signal is gated in the A-FL unit to produce SHO (Store Heaters ON) which is used to turn on the power amplifier for the store heaters (VT17, 18 and 19).

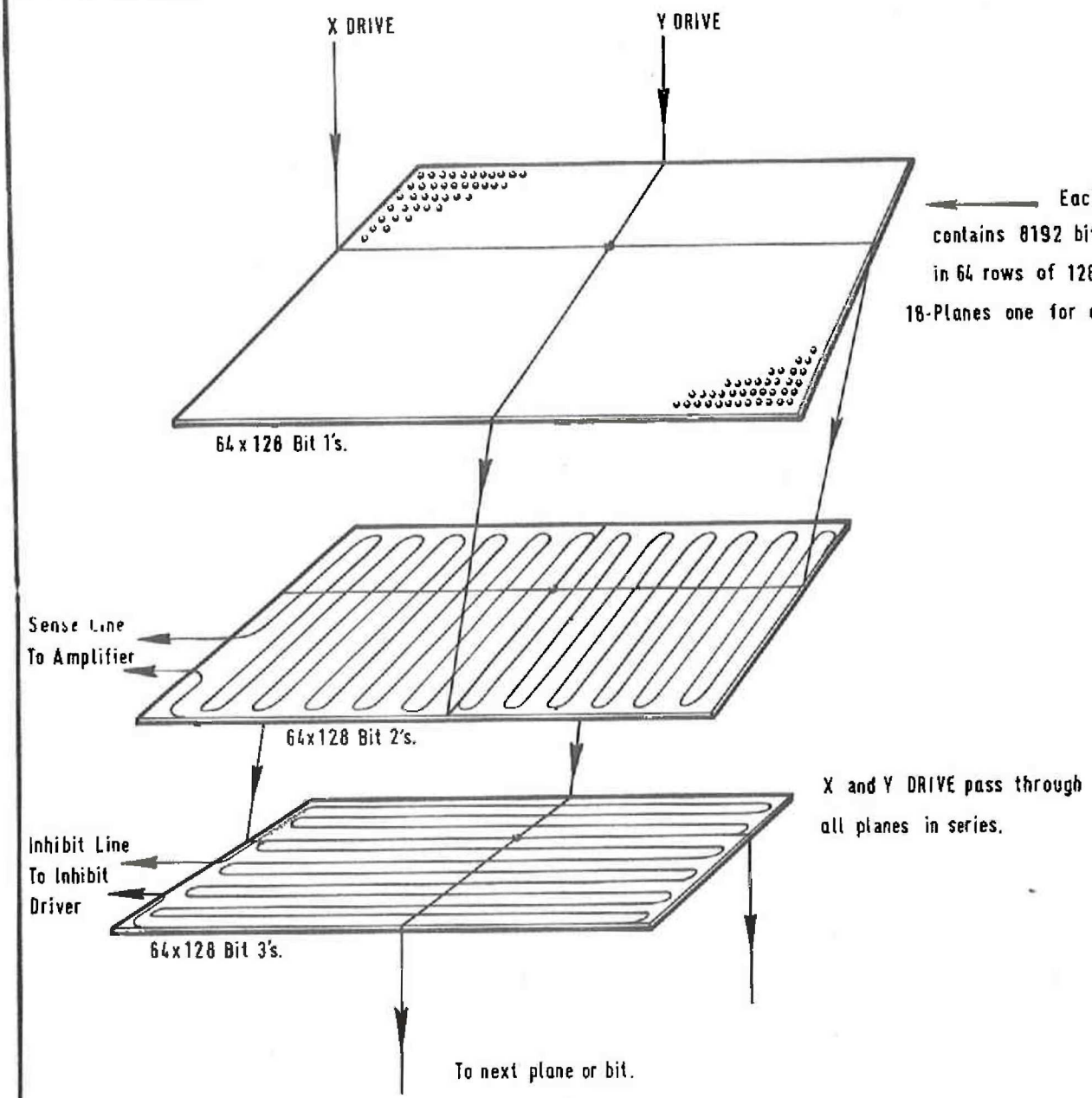
Note: Store heaters are only available on MCB 2 computers.

11.3.3 Store Heater Off and Restart Circuit (MCB 2 computers only)

The purpose of this circuit is to switch-off the store heaters when the store temperature is at about -5°C. It comprises VT9, VT10, VT11 and associated resistors, capacitor and Zener diodes.

If the temperature rises from -15°C towards 0°C, the reference voltage will fall from 9.9V. When the reference reaches 9.6V, VT10 will switch-on VT9. This will trigger SCR VT21 and leave it on after removal of the trigger.

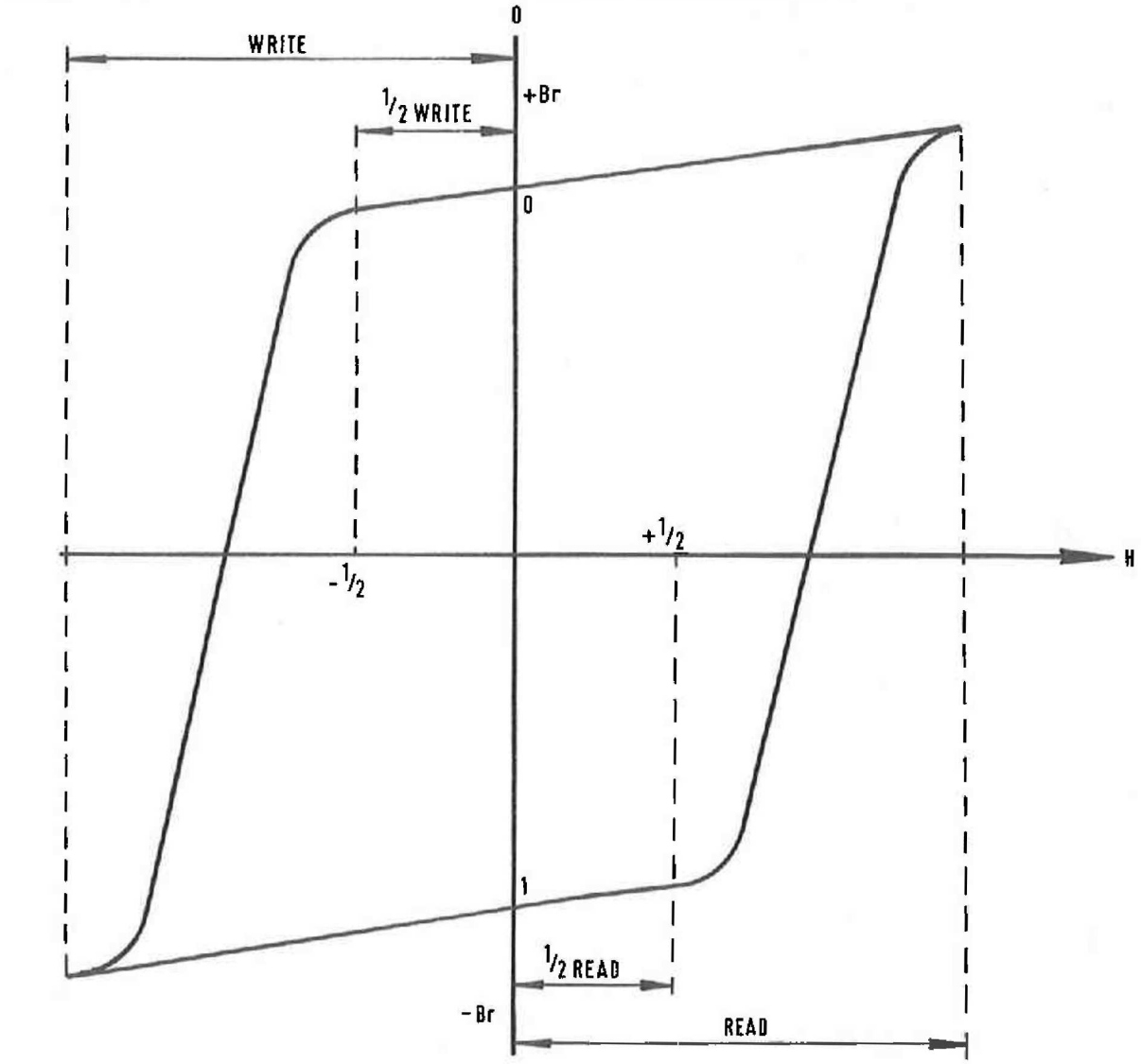
The anode of VT21 which is at +6V in the off condition goes rapidly to 0V. The 6V negative going pulse is passed via C5 and C6 to the anode of VT22 switching it off, VT20 is then switched on and VT23 switched off sending the logic signal STC (Store Temperature Correct) to the A-FL logic board. This switches off the store heaters and allows the computer to be started in the normal manner.



Each core has passing through it:-

1. An X Line.
2. A Y Line.
3. An Inhibit line (Write).
4. A Sense line.

Fig n. Core Stack. ISS. 1.



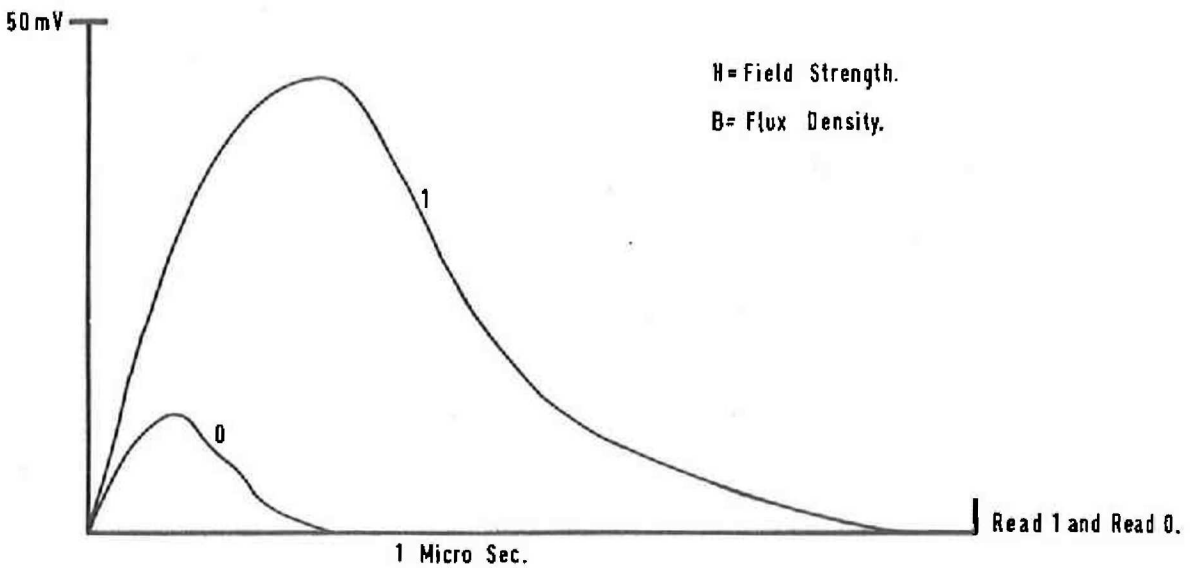


Fig o. Switching Response of Ferrite Core.

ISS. 1.

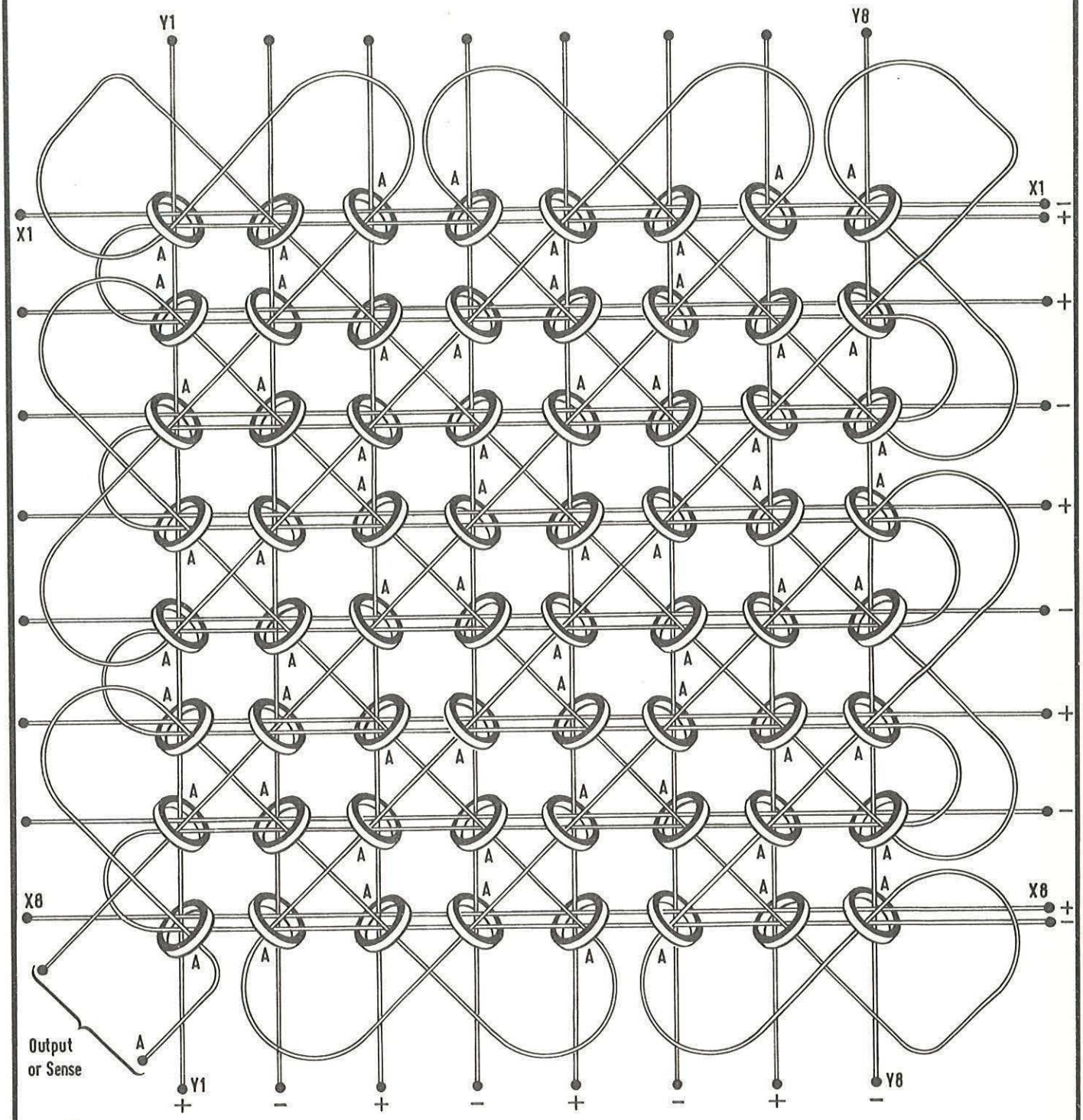
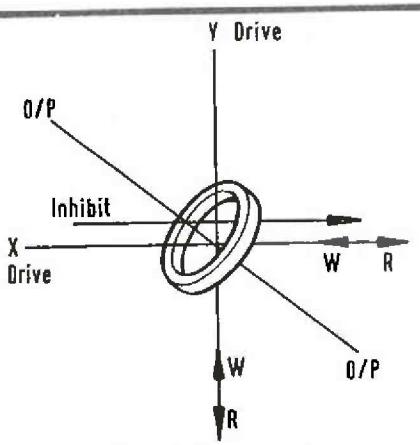
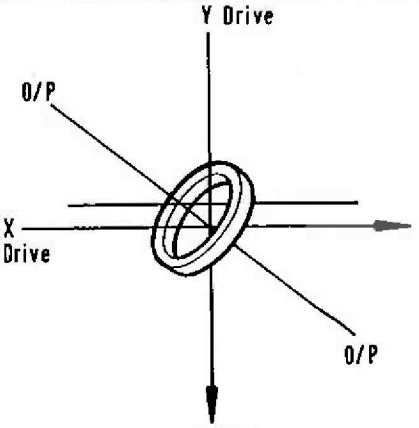


Fig p. Diagonal Thread Pattern.

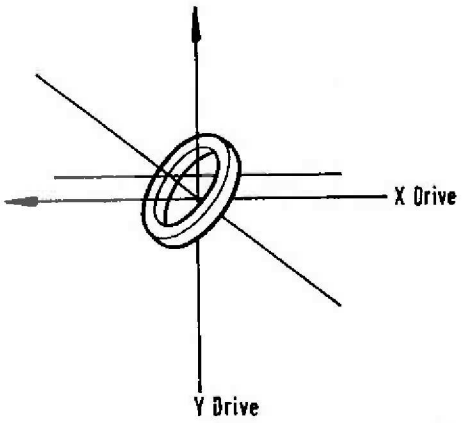
ISS. 1.



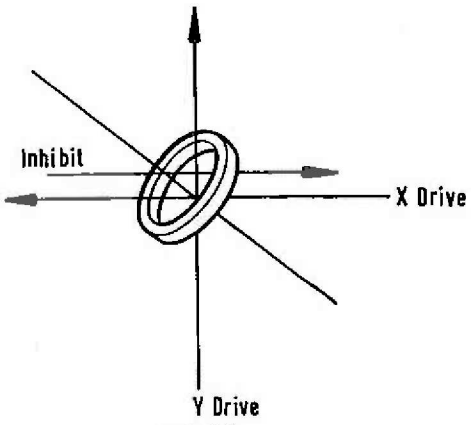
General Arrangement



Read '1' or '0'

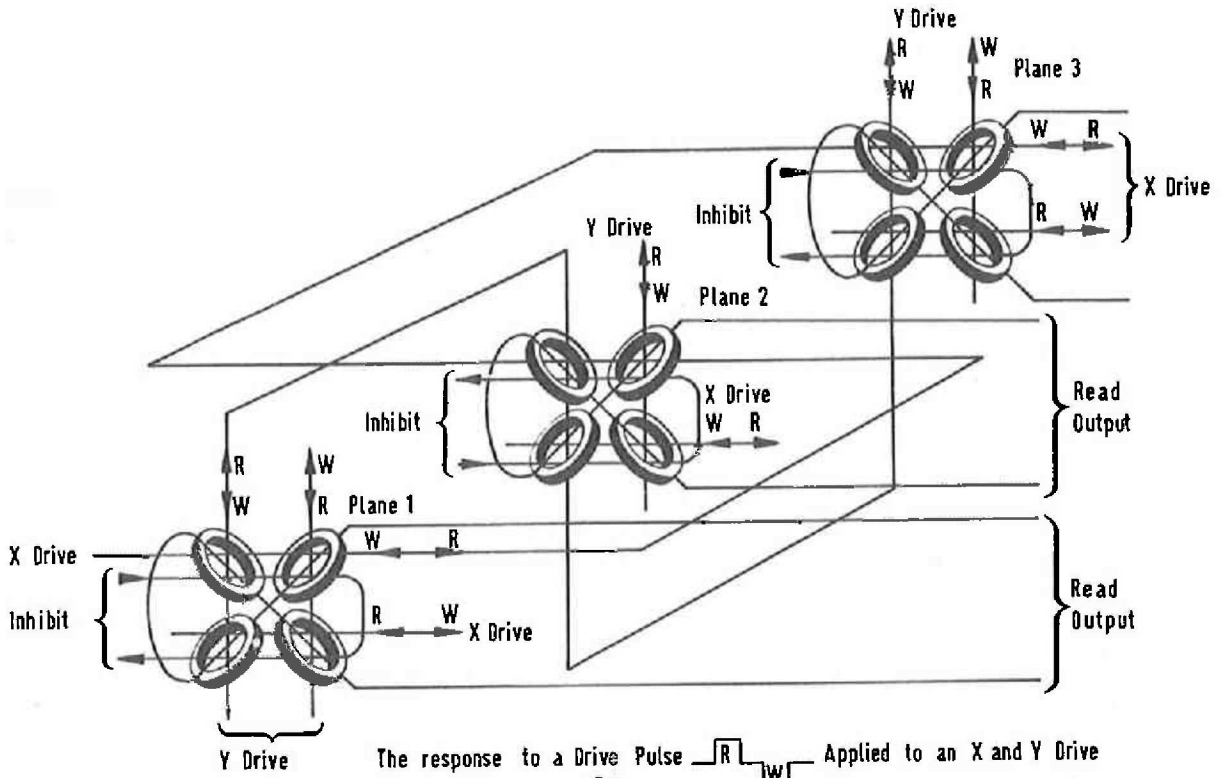


Write '1'



Write '0'

Core Detail Fig.q.



The response to a Drive Pulse ⎍R⎍W⎍ Applied to an X and Y Drive Wire will appear as ∩R∪W at the Sense Winding of each Plane unless Inhibited sense Response in the Inhibited Plane will be ∩∪

Detail of Core Selection and Drive for locations in three Planes Fig. r. ISS. 1.

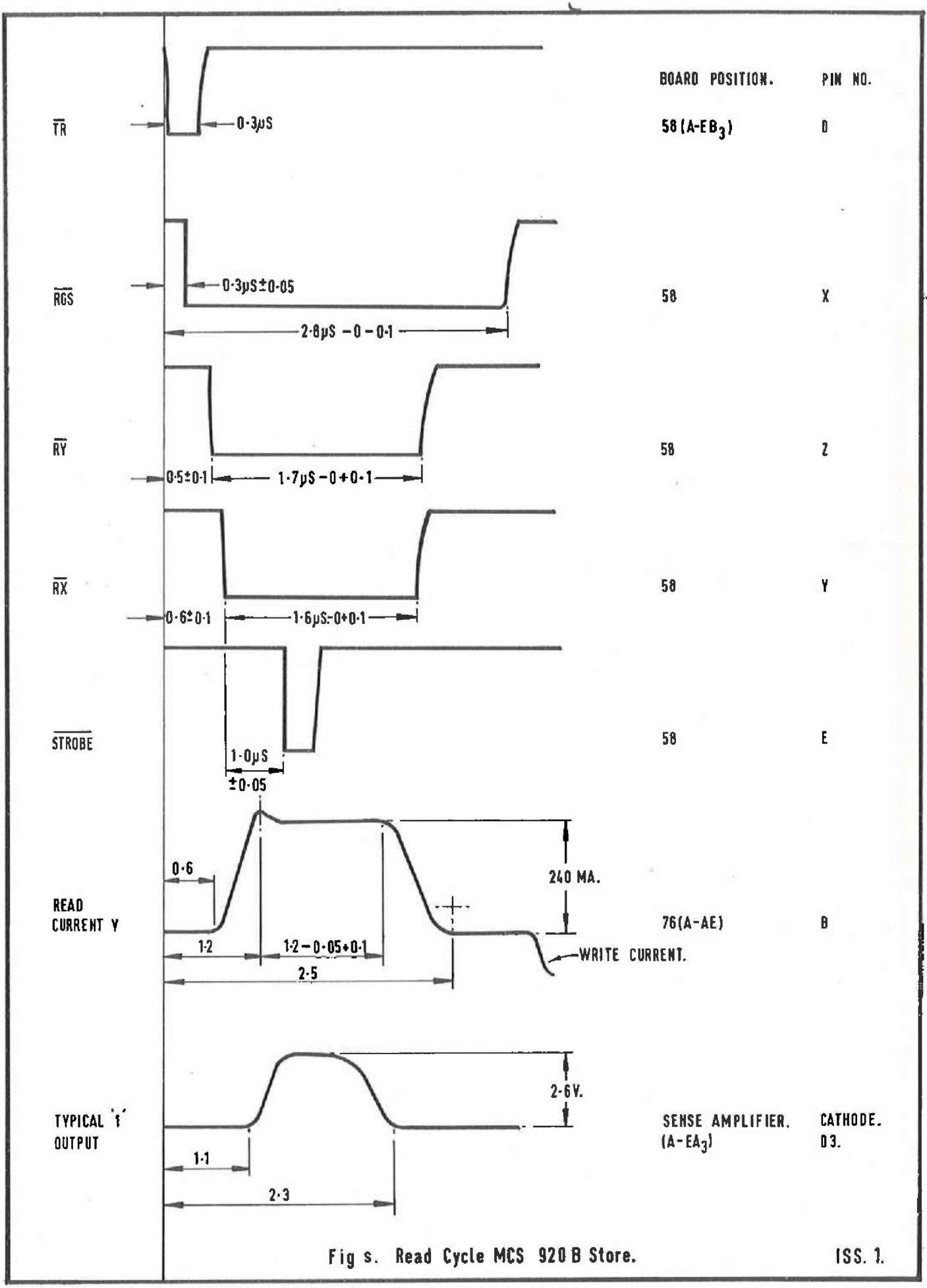


Fig s. Read Cycle MCS 920 B Store. ISS. 1.

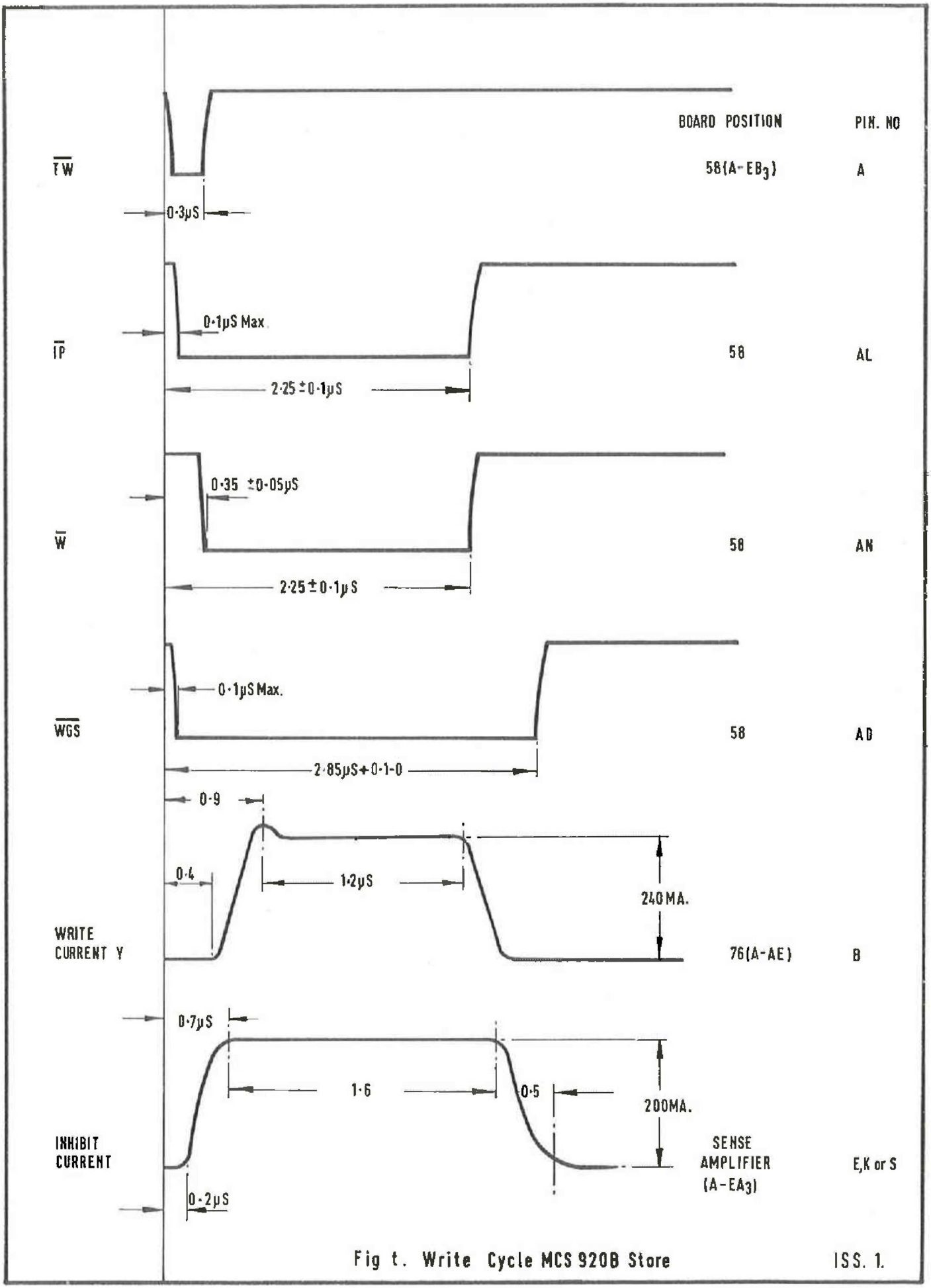


Fig t. Write Cycle MCS 920B Store ISS. 1.

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE NO. MCB 143

PART 1: CENTRAL PROCESSOR

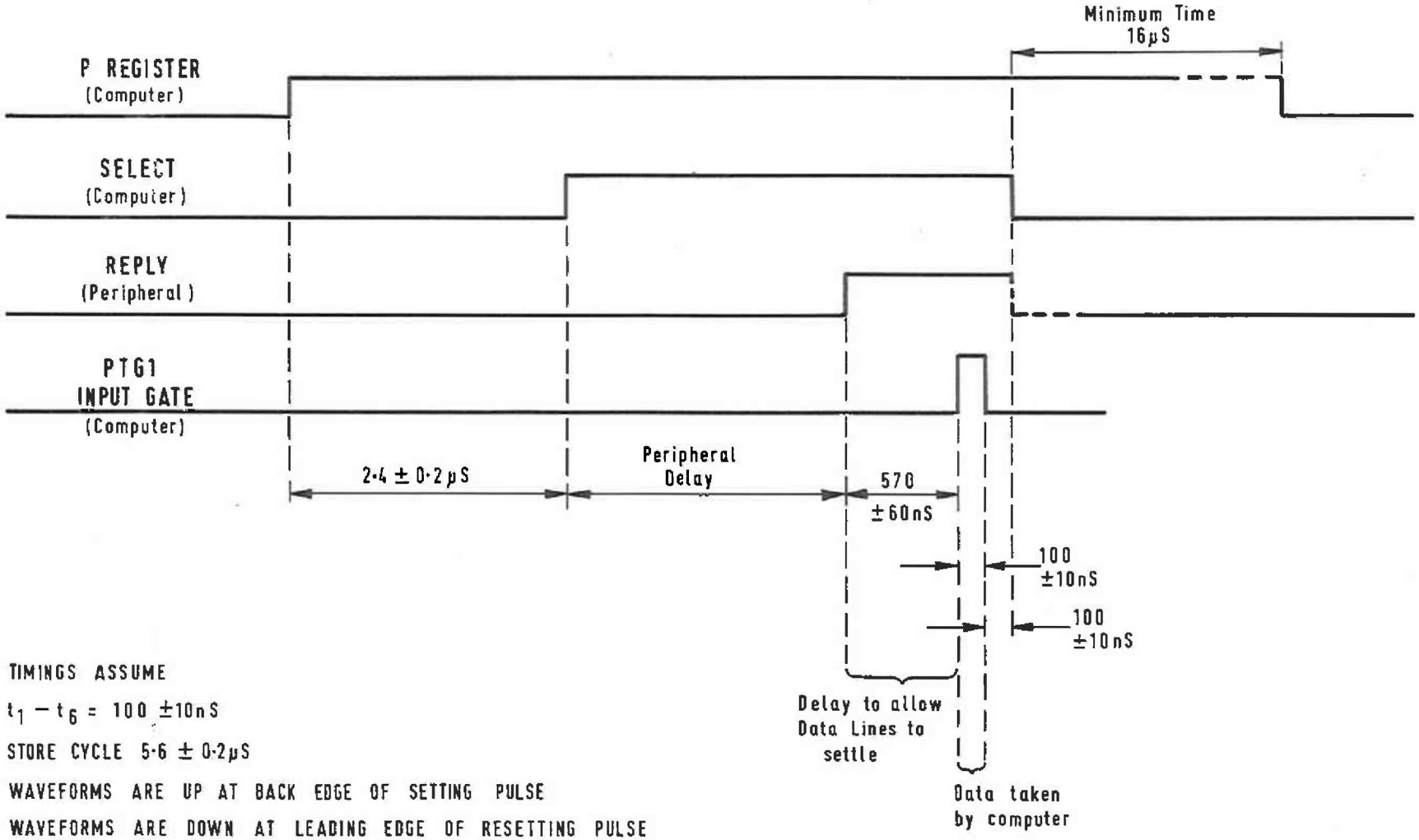
CHAPTER 6: INTERFACE

CHAPTER 6

INTERFACE

CONTENTS

LIST OF FIGURES



TIMINGS ASSUME

$t_1 - t_6$ = 100 ±10nS

STORE CYCLE 5·6 ± 0·2μS

WAVEFORMS ARE UP AT BACK EDGE OF SETTING PULSE

WAVEFORMS ARE DOWN AT LEADING EDGE OF RESETTING PULSE

Fig. u. Direct Input Timing

ISS. 1.

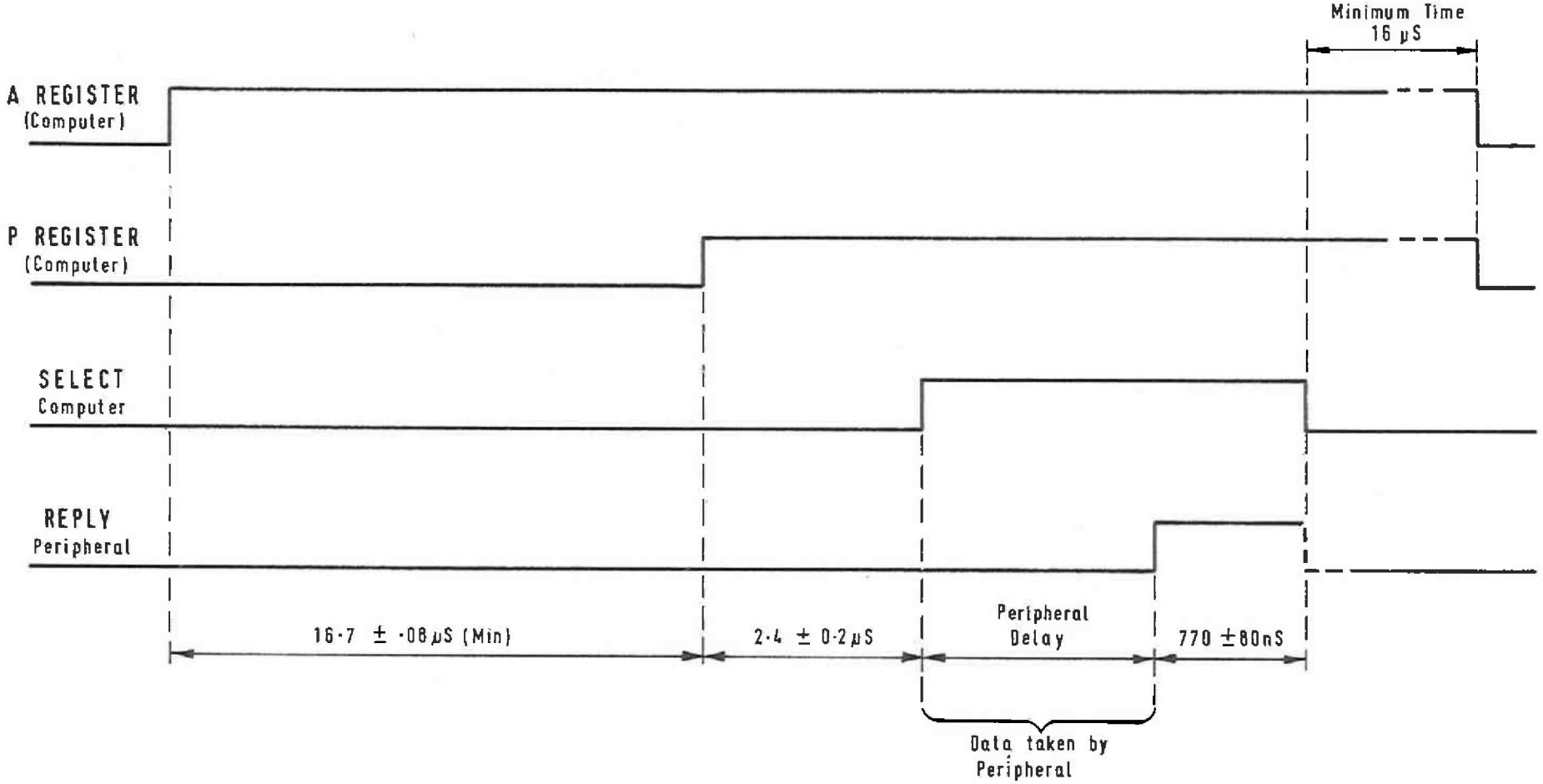


Fig. v. Direct Output Timing

ISS. 1.

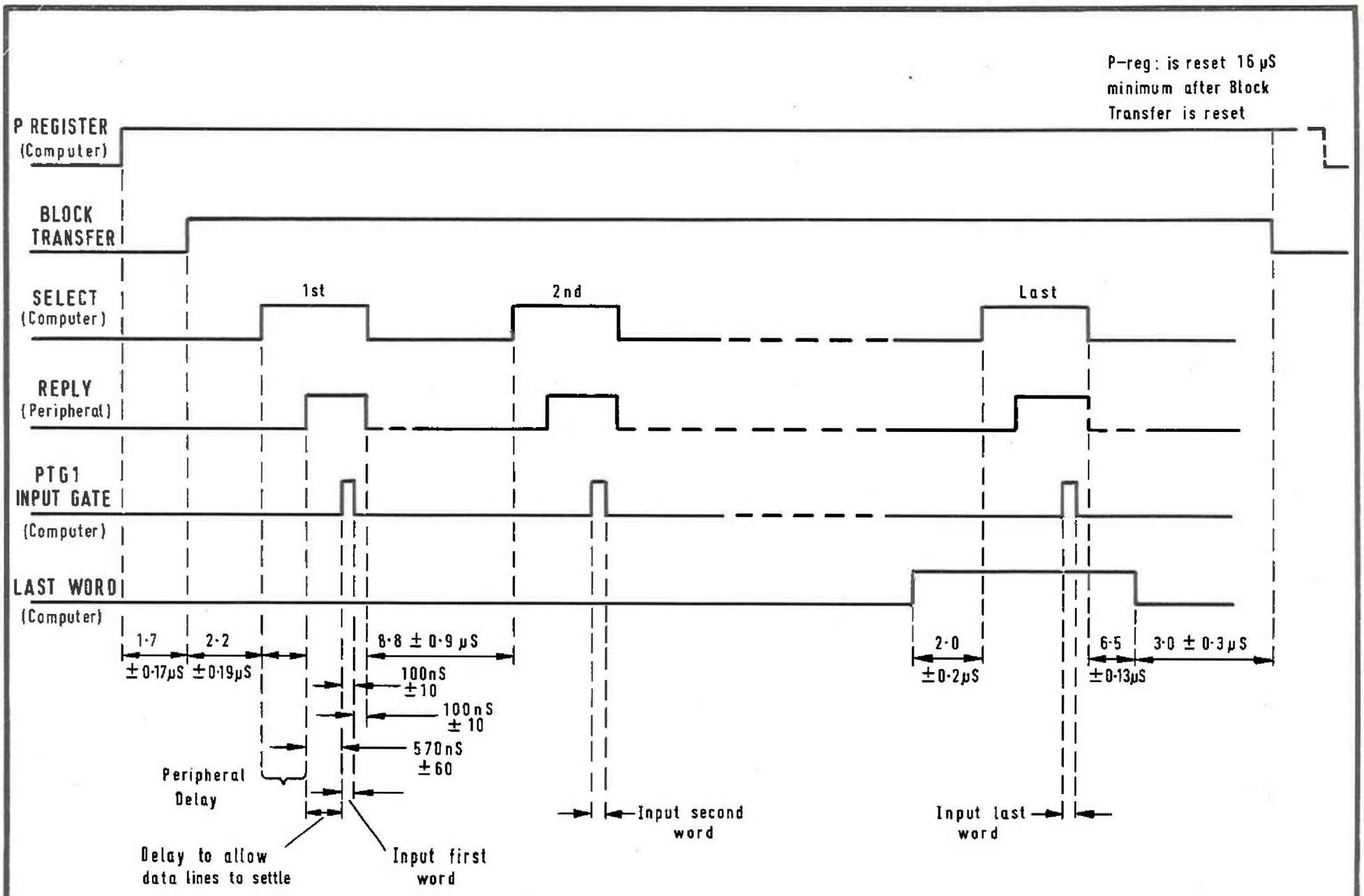


Fig. w. Block Input Timing

ISS. 1.

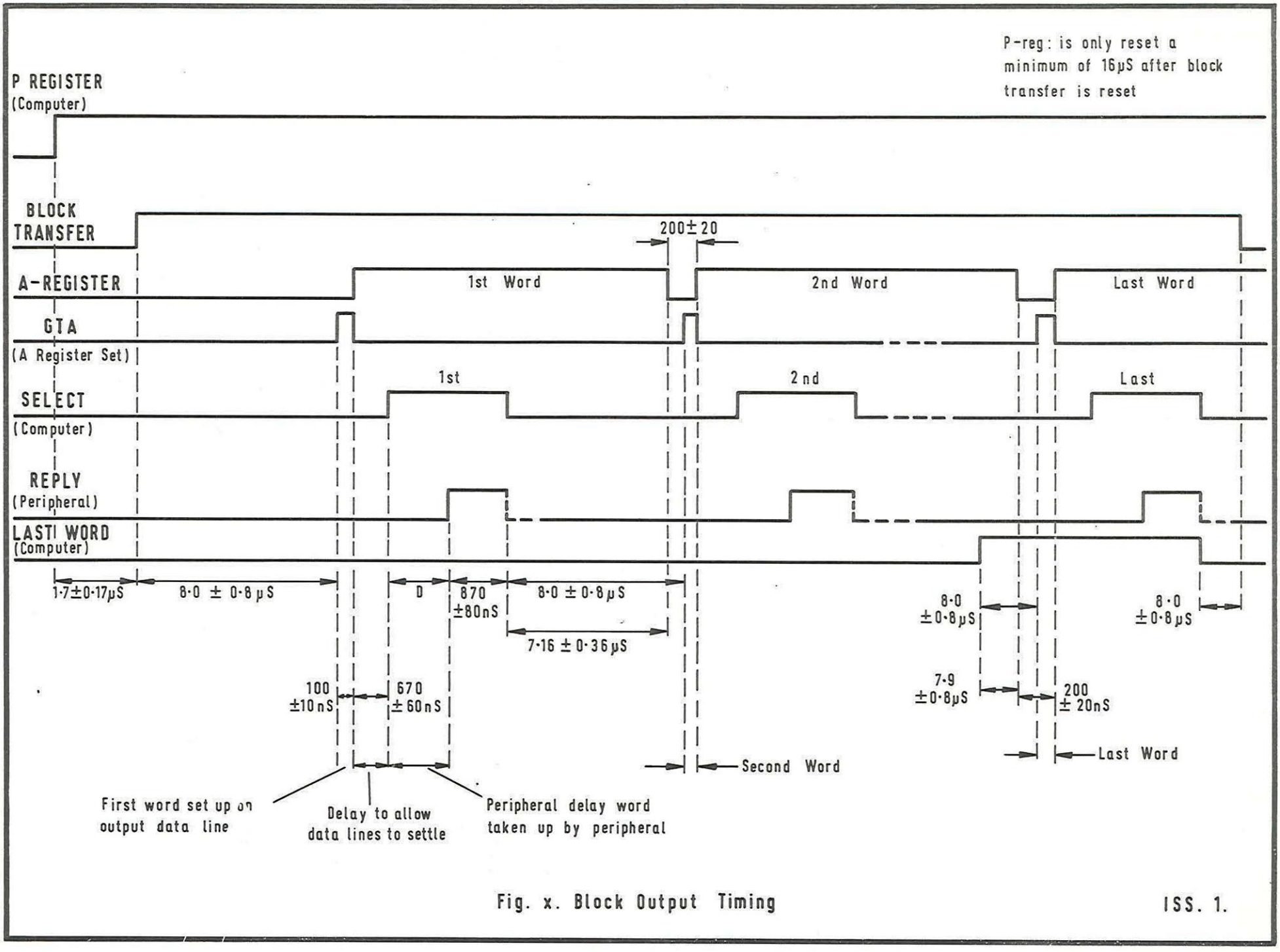


Fig. x. Block Output Timing

ISS. 1.

CHAPTER 6

INTERFACE

1. SCOPE OF INPUT AND OUTPUT INSTRUCTIONS

The functions available for the transfer of data between computer and peripheral are as follows:

1.1 Direct Input 15 N where $0 \leqslant N \leqslant 2047$

During this instruction one 18 digit word is transferred from the peripheral device specified by N to the computer.

1.2 Direct Output 15 N where $4096 \leqslant N \leqslant 6143$

During this instruction one 18 digit word is transferred from the computer to the peripheral device specified by N.

1.3 Block Input 14 N where $2048 \leqslant N \leqslant 4095$

During this instruction a number of 18 digit words are transferred from the peripheral device specified by N, to the computer. The actual number of words transferred depends on the state of two registers within the computer, which must be set up using other instructions before the block input instruction is obeyed.

1.4 Block Output 14 N where $4096 \leqslant N \leqslant 6143$

During this instruction a number of 18 digit words are transferred from the computer to the peripheral device specified by N. The number of words transferred is as described for block input.

1.5 Paper Tape, Program Terminate and Shift Instructions

It may be noted that functions 14 and 15 initiate other effects when 'N' is outside the ranges stated above. These are summarized as follows, but have no effect at socket 13, which carries the control waveforms to and from external peripherals.

(a) 14 N where $0 \leqslant N \leqslant 2047$ - Left shift N places.

(b) 14 N where $6144 \leqslant N \leqslant 8191$ - Right shift (8192-N) places.

(c) 15 N where $2048 \leqslant N \leqslant 2063$ - Reader input and control.

(d) 15 N where $6144 \leqslant N \leqslant 6159$ - Punch output and control.

(e) 15 N where $7168 \leqslant N \leqslant 8191$ - Program terminate.

From the ranges of N stated above it will be seen that up to 2048 separate input devices and 2048 separate output devices can be addressed directly. The eleven least significant binary digits of the peripheral address are available on socket 4 which are termed OSn (where n = 1 to 11) for decoding as necessary. Inputs and outputs are then determined by the appropriate select signal.

A single set of input and output connections is provided, all information to be transferred is multiplexed on to these connections and arrangements for correct routing of information must be made in any system of peripheral devices.

A synchronous control system is used, so that the computer can communicate with devices of any speed.

2. INTERFACE SIGNALS ON SOCKETS 4 and 13

The following is a description of the signals present at the input/output sockets, in the order in which they are activated during the

time that an input or output function is being obeyed by the computer. Socket 4 contains the data and peripheral address lines whilst socket 13, the control waveforms needed to initiate date transfer. The waveforms are summarized in the timing diagrams given in section 5.

2.1 Direct Input

At the beginning of the function the peripheral address lines (OS_n, n = 1-11) are set up to the least significant eleven digits of the binary equivalent of the address N, specifying the particular input peripheral required. After this, the select input peripheral (SIP) line goes true and the computer will wait for the peripheral reply (PR) line to go true indicating that the peripheral selected is ready to transfer information to the computer. This information must be available on the data input lines (IG_n, n = 1 to 18) before PR goes true, and as an added precaution, there is a delay of approximately 500ns between the reception of PR by the computer and the actual input of that data into a computer register. This delay serves two purposes.

(a) It ensures, as far as the computer is concerned, that the data lines have had sufficient time to settle to either a true or false state.

(b) PR signals of less than 500ns duration are rejected. This ensures that spurious noise spikes on the peripheral reply line do not initiate the input of incorrect data.

After the data has been transferred to the computer, the select input signal is returned to the false state and this "back edge" may be used to return the peripheral reply signal also to the false state. In any case PR must be set false before the next input (or output) instruction is attempted.

2.2 Direct Output

The data output lines (OA_n, n = 1 to 18) will have been set up during an earlier instruction obeyed by the computer. At the beginning of a direct output instruction, the peripheral address lines will be set up and then the select output peripheral (SOP) line will go true. The computer will then wait until the peripheral reply line goes true indicating that the output peripheral specified has taken up the information on the data output lines. Approximately 770ns after PR has gone true (and provided PR is longer than 500ns), the select signal is returned to the false state and again this "back edge" may be used to return PR also to the false state.

It should be noted that if an output or input select signal is sent out by the computer, but no reply is received (as in the case when a non-existent peripheral is addressed) the computer will be held up indefinitely.

2.3 Block Input

The block input function allows direct transfer of information between an input peripheral device and successive locations of the computer store. The number of words transferred and the computer store locations into which the words are written, depends on the contents of two registers in the computer which must be set up by program action before a block input function is attempted.

After the peripheral address lines have been set up, the block transfer (BT) line will go true, indicating to the peripheral system that a block transfer is about to take place. The first select input peripheral signal is then generated then, as in direct input, the computer waits for the peripheral reply line to go true, before inputting the data on the data input lines. After this has occurred the select signal is returned to the false state, and there is a delay of approximately 8 μs before the

select input signal goes true again, ready to input the second word. During this delay, the first word taken in is written into the computer store. The peripheral reply line must be true for longer than 500ns, but must be returned to the false state before the select signal is set true for the next word.

Just before the select signal is set true for the final word transfer, the last word (LW) line goes true indicating to the peripheral system the completion of the block input function. The final word is then sensed and written into the store. After the select signal has returned to the false state, the last word and then block transfer lines are returned to the false state at approximately 6.5 and 3.0 respectively.

2.4 Block Output

The block output function allows direct transfer of information between successive locations of the computer store and an output peripheral device. The number of words transferred and the computer store locations from which these words are read, depends on the contents of two registers in the computer which must be set up by program action before a block output function is attempted.

After the peripheral address lines have been set up, the block transfer line will go true. The data output lines are then set up to the first store word to be output and after a delay to allow these lines to settle, the first select output peripheral signal is generated. As in direct output, the computer will wait for the peripheral reply line to go true, indicating that the first word has to be taken up by the peripheral system. 870ns (approximately) after peripheral reply has gone true (and provided peripheral reply is longer than 500ns) the select signal returns to the false state and remains so for a delay of 8μs. During this delay the peripheral reply line must be returned to the false state and also the second

word is read from the store and set up on the data output lines.

Just before the select signal is set true for the final word transfer, the last word line is made true. The final word of data is available for output whilst select is true. The select and last word lines are set false approximately at the same time, with the block transfer line being made false approximately 8.0 μs later.

3. SUPPLEMENTARY SIGNALS

Other signals on the input/output sockets not mentioned above are:

(a) COMPUTER ON - wired directly to the computer +6V rail.

(b) RESET - true when computer is in reset state. This occurs when:

(i) The computer is first switched on but the program has not yet been triggered.

(ii) The reset button is pressed on the control unit

(iii) The computer is switched off.

(iv) The ambient temperature exceeds the specified temperature range whilst the computer is running.

(c) PERIPHERAL INTERRUPTS (PI_1, PI_2, PI_3) - these lines normally held in the false state, may be set true to initiate action of the computer priority program system. They must be held in the true state for a minimum time of 10μs or < 75μs (maximum) unless reset by program.

4. INTERFACE CIRCUITS

4. 1 Data, Peripheral Address and Reset

Data out, (OA_n), Peripheral Address (OS_n), Data in (IG_n) and Reset.

These waveforms appear on socket 4. The data out, peripheral address and reset lines are the outputs from cable transmitters which must be terminated by cable receivers at the peripheral system end of the cable, which the data in lines are the inputs to cable receivers which must be driven at the peripheral system end of the cable by cable transmitters. The general system of transmitter/receiver is as shown by Fig. y.

Ringing on the cable when the transmitter is set limits the length of cable to 20' maximum.

4. 2. Voltage levels in true and false states

4. 2. 1 Unloaded transmitter - the signal levels at 'A' relative to computer zero volts (0V) for an unloaded transmitter are:

Output levels — Transmitter OFF $V_o = +6V \pm 0.5V$

Transmitter ON $V_o = 0V^{+0.4V}_{-0}$ unloaded

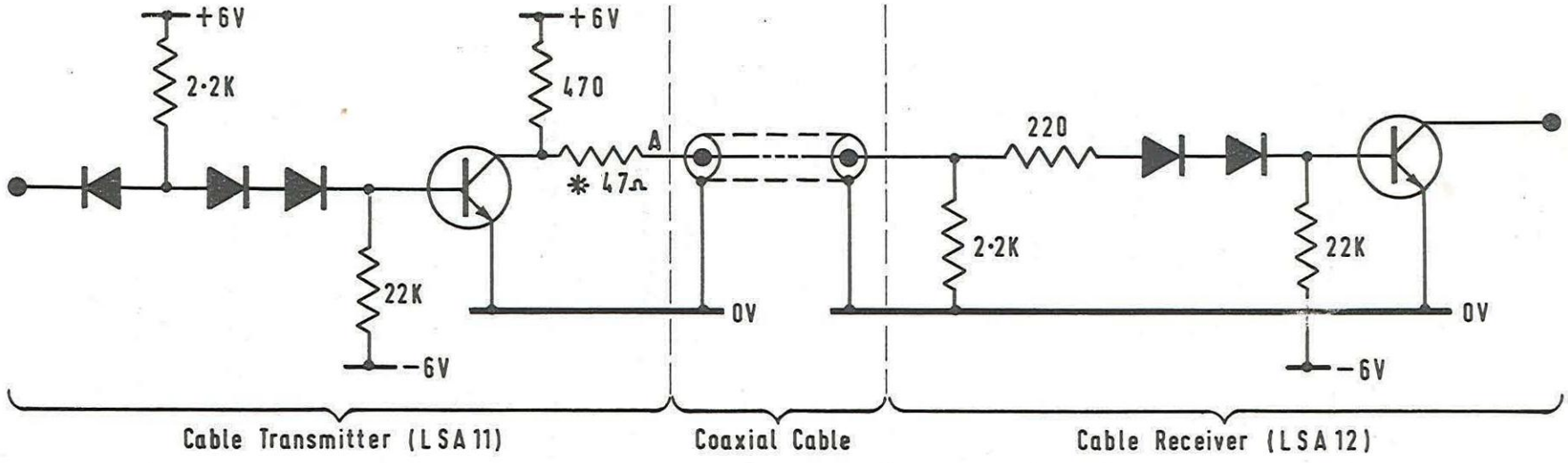
VT1 is to 322PURCH 100 (2N2369A type)

All diodes to 322PURCH 101 (1S44 type)

4. 2. 2 Transmitter/receiver combination - the voltages on the 'line' in the true and false states are as follows:

Transmitter OFF V_o = 3. 2V nominal

Transmitter ON V_o = 0V + 1. 7V



* Note: TX. 47Ω series resistor only fitted on control lines

Fig. y. Cable Transmitter and Receiver (LSA 11 and 12)

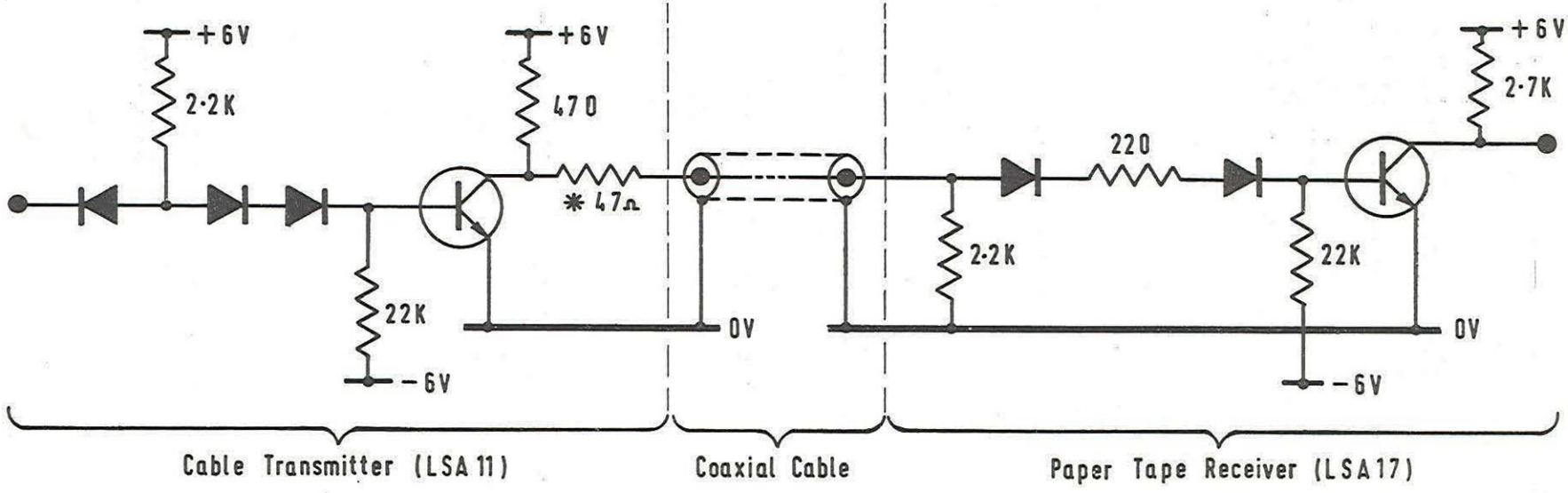


Fig. z. Cable Transmitter and Paper Tape Receiver (LSA 11 and 17)

ISS. 1.

Earthing - the cable on socket 4 should be screened overall and connected at both ends to computer zero volts.

Mains earth is brought out to a pin so that computer and peripheral chassis may be connected together.

4.3 Control waveforms

These waveforms all appear on socket 13. The select output peripheral, select input peripheral, block transfer and last word lines are the outputs from cable transmitters which must be terminated by cable receivers at the peripheral system end of the cable, whilst the peripheral interrupts 1, 2 and 3, and peripheral reply lines are the inputs to cable receivers which must be driven at the peripheral system end of the cable by cable transmitters. Coaxial cable is used in the interconnection between computer and peripherals to avoid spurious pick-up on these control lines and they must be matched at the transmitter end by a 47 Ω resistor in series with the output. The general system of transmitter/receiver is as shown by Fig. y.

4.4 Paper Tape Transmitters and Receivers

Used for Tape reader input and Tape punch output on socket 10.

Cable Transmitter (LSA 11)

Loading: one cable and one receiver to each transmitter.

Output levels: Transmitter OFF $V_o = 6V \pm 0.5V$) unloaded
Transmitter ON $V_o = 0V \begin{smallmatrix} +0.4V \\ -0 \end{smallmatrix}$) unloaded

If connected to Cable Receiver, fig. z (LSA 17)

Transmitter OFF $V_o = 3.2V$ nominal
Transmitter ON $V_o = 0V \begin{smallmatrix} +1.7V \\ -0 \end{smallmatrix}$

Cable Receiver

Used to terminate all cables carrying signals from the tape reader.

Input Level

To switch Receiver OFF $0 < V_s < 1.7V$

To switch Receiver ON $2.6 < V_s < 6.5V$

Transmitter and receiver circuit is shown in Fig. z.

5. TIMING DIAGRAMS

The sequence of interface signals described in section 2 are summarized in diagrams u, v, w and x shown on Page 1, 2, 3 and 4.

6. INTERCONNECTIONS

All connections to the computer are made via the plugs and sockets listed.

Socket 1.	Display Unit
Socket 2.	Display Unit
Socket 3.	Display Unit
Socket 4.	Input/Output (data)
Socket 5.	Control Unit
Plug 6.	Power Supply Unit
Socket 7.	Margin Test Unit
Socket 8.	Additional Store
Socket 9.	Additional Store
Socket 10.	Paper Tape Controller.
Socket 11.	Control Unit
* Plug 12.	Blower Supply
Socket 13.	Input/Output (Control)
Socket 14.	Additional Store

* Used on early machines only

The list of notes shown below refer to the appropriate tolerances, which appear in the tolerance column of the following interconnection tables.

Note 1

(With 3.9k limiting resistor and no pull up)

The voltages are measured using a 10 kΩ resistor connected between the pin and +6V and the display unit disconnected.

True state will be +6V ± 10% ('0') Impedance 3.9 kΩ

False state will be +2V ± 10% ('1') Impedance 7 kΩ

These are bar outputs, hence '0' and '1' are interchanged.

Note 2

(With 3.9k limiting resistor and 1 kΩ pull up or 2.2 kΩ pull up)

The voltages are measured using a 10 kΩ resistor connected between the pin and +6V and the display disconnected.

True state will be +6V ± 10% ('0') Impedance 3.9 kΩ

False state will be +2V ± 10% ('1') Impedance 5 kΩ

These are bar outputs, hence '0' and '1' are interchanged.

Note 3

True signal levels will be $>$ +2 V and $\leqslant$ +6V ('1')

Impedance 470Ω

False signal levels will be $<$ +1 V and $\geqslant$ 0V ('0')

Impedance 5Ω

Any voltage levels outside these specified limits will be fault or transient conditions.

Note 4

True signal levels will be $>$ +2 V and $<$ +6V ('1')

Impedance 1 kΩ

False signal levels will be $< +1$ V and ≥ 0 V ('0')

Impedance 470 Ω

Any voltage levels outside these specified limits will be fault or transient conditions.

Note 5

True signal levels will be $> +2.3$V and $< +6$ V ('1')

Impedance 470 Ω

False signal levels will be $< +1$ V and ≥ 0 V ('0')

Impedance 5 Ω

Any voltage levels outside these specified limits will be faults or transient conditions.

Note 6

Temperature dependent reference voltage will be 8.65V at 25°C which will change by - 0.45% (26 millivolts and < 3mA load) for every degree centigrade drop in temperature and (26 millivolts and < 3mA load) for every degree centigrade rise in temperature.

Note 7

The voltages are measured using a 470 Ω resistor connected between the pin and 0V.

True state will be 4.5V ± 1 V ('1')

False state will be 0V ± 0.5V ('0')

Any voltage levels outside these specified limits will be fault or transient conditions.

Note 8

True signal levels will be $> +2$V and $\leq +6$V ('1')

Impedance 520 Ω

False signal levels will be $< +1$V and ≥ 0V ('0')

Impedance 50 Ω

Any voltage level outside those specified will be fault or transient conditions.

Note 9

Computer 0V is isolated from chassis.

Note 10

The maximum current required from the +6V supply is 10.0 amps. The voltage (at 25^{0}C and 8.0 amps) as measured at input to the computer (MCB 2) should be 6.0V ± 5% and stable to ± 2% over the temperature range - 10^{o}C to +55^{o}C. The static regulation should not exceed 10% from 4.0 amps to 8.0 amps, as measured at the computer. The maximum ripple voltage should never exceed 150mV peak-to-peak.

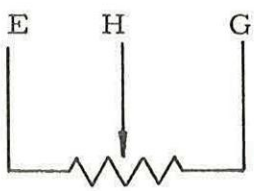
The - 6V supply must be capable of delivering a maximum current of 2.0 amps. The voltage (at 25^{o}C and 2 amps) as measured at input to the computer (MCB 2) should be - 6.0V ± 5% and stable to ± 2% over the temperature range - 10^{o}C to +55^{o}C.

The static regulation should not exceed 6% from 1 amp to 2 amps.

The maximum ripple voltage should never exceed 100mV peak-to-peak.

Note 11

Skt 7



8.65V
Note 6

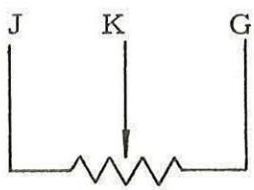
0V
Note 9

This circuit is used for the Drive current margins

5 kΩ

Note 12

Skt 7



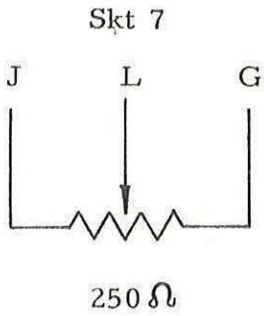
6V
Note 10

0V
Note 9

This circuit is used for the Main Timing loop

500Ω

Note 13



6V Note 14

0V Note 9

This circuit is used for the Pulse Generator Margins

Note 14

15V d. c. at 25°C will have a full load current of 2. 0 amps. The voltage decrease per degree centigrade rise in temperature will be approximately - 0. 45%. Maximum ripple voltage at full load 150mV peak-to-peak. Static regulation between 0. 1 amp , and 2. 0 amps, should not exceed 2% measured at the computer.

Note 15

- 16V ± 10% 30mA supply is an unstabilised bias supply for Extra Stores circuits.

Note 16

240V ± 10% and 50 c/s to 60 c/s single phase.

Note 17

Nominal 24/28V supply will be between 20V and 34V (floating). Further details will be defined at a later date.

SOCKET SKT 1 DEF. 5325/3. TYPE: THORNE PT00E 24-61 SW (Computer to Display Unit)
MATING FREE PLUG DEF. 5325/3. TYPE: THORNE PT06E 24-61 PW

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH				CABLE SCREEN	Chassis	Bolt Tag
B	MONITOR G_1	(G_1)	OUT	NOTE 1		56	M
C	" G_2	(G_2)	OUT	"		55	M
D	" G_3	(G_3)	OUT	"		54	M
E	" G_4	(G_4)	OUT	"		53	M
F	" G_5	(G_5)	OUT	"		52	M
G	" G_6	(G_6)	OUT	"		51	M
H	" G_7	(G_7)	OUT	"		50	M
J	" G_8	(G_8)	OUT	"		49	M
K	" G_9	(G_9)	OUT	"	G REGISTER DIGITS	48	M
L	" G_{10}	(G_{10})	OUT	"		45	M
M	" G_{11}	(G_{11})	OUT	"		44	M
N	" G_{12}	(G_{12})	OUT	"		43	M
P	" G_{13}	(G_{13})	OUT	"		42	M
R	" G_{14}	(G_{14})	OUT	"		41	M
S	" G_{15}	(G_{15})	OUT	"		40	M
T	" G_{16}	(G_{16})	OUT	"		39	M
U	" G_{17}	(G_{17})	OUT	"		38	M
V	" G_{18}	(G_{18})	OUT	"		37	M

SOCKET SKT 1 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
W	MONITOR A_1	(A_1)	OUT	NOTE 2	A REGISTER DIGITS	56	Z
X	" A_2	(A_2)	OUT	"		55	Z
Y	" A_3	(A_3)	OUT	"		54	Z
Z	" A_4	(A_4)	OUT	"		53	Z
a	" A_5	(A_5)	OUT	"		52	Z
b	" A_6	(A_6)	OUT	"		51	Z
c	" A_7	(A_7)	OUT	"		50	Z
d	" A_8	(A_8)	OUT	"		49	Z
e	" A_9	(A_9)	OUT	"		48	Z
f	" A_{10}	(A_{10})	OUT	"		45	Z
g	" A_{11}	(A_{11})	OUT	"		44	Z
h	" A_{12}	(A_{12})	OUT	"		43	Z
i	" A_{13}	(A_{13})	OUT	"		42	Z
j	" A_{14}	(A_{14})	OUT	"		41	Z
k	" A_{15}	(A_{15})	OUT	"		40	Z
m	" A_{16}	(A_{16})	OUT	"		39	Z
n	" A_{17}	(A_{17})	OUT	"		38	Z
p	" A_{18}	(A_{18})	OUT	"		37	Z

SOCKET SKT 1 (Contd) (Computer to Display Unit)

	WAVEFORM		IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION	
PIN REF	TITLE	ABBREV.				BOARD POSN.	PIN
q	MONITOR Q_1	(Q_1)	OUT	NOTE 1	Q REGISTER DIGITS	56	AC
r	" Q_2	(Q_2)	OUT	"		55	AC
s	" Q_3	(Q_3)	OUT	"		54	AC
t	" Q_4	(Q_4)	OUT	"		53	AC
u	" Q_5	(Q_5)	OUT	"		52	AC
v	" Q_6	(Q_6)	OUT	"		51	AC
w	" Q_7	(Q_7)	OUT	"		50	AC
x	" Q_8	(Q_8)	OUT	"		49	AC
y	" Q_9	(Q_9)	OUT	"		48	AC
z	" Q_{10}	(Q_{10})	OUT	"		45	AC
AA	" Q_{11}	(Q_{11})	OUT	"		44	AC
BB	" Q_{12}	(Q_{12})	OUT	"		43	AC
CC	" Q_{13}	(Q_{13})	OUT	"		42	AC
DD	" Q_{14}	(Q_{14})	OUT	"		41	AC
EE	" Q_{15}	(Q_{15})	OUT	"		40	AC
FF	" Q_{16}	(Q_{16})	OUT	"		39	AC
GG	" Q_{17}	(Q_{17})	OUT	"		38	AC
HH	" Q_{18}	(Q_{18})	OUT	"		37	AC

SOCKET SKT 1 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
JJ	MONITOR X OVERFLOW	(X)	OUT	NOTE 1	OVERFLOW BISTABLES	57	D
KK	MONITOR Y OVERFLOW	(Y)	OUT	"		57	Z
LL	MONITOR SELECT OUTPUT PERIPHERAL	(SOP)	OUT	"		30	P
MM	MONITOR SELECT INPUT PERIPHERAL	(SIP)	OUT	"		30	Z
NN	MONITOR SELECT TAPE PUNCH	(STP)	OUT	"		30	L
PP	MONITOR SELECT TAPE READER	(STR)	OUT	"		30	H

SOCKET SKT 2 DEF.5325/3 TYPE: THORNE PT00E 24-61 SX (Computer to Display Unit)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 24-61 PX

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH				CABLE SCREEN	Chassis	Bolt Tag
B	MONITOR M_1	(M_1)	OUT	NOTE 2		56	U
C	" M_2	(M_2)	OUT	"		55	U
D	" M_3	(M_3)	OUT	"		54	U
E	" M_4	(M_4)	OUT	"		53	U
F	" M_5	(M_5)	OUT	"		52	U
G	" M_6	(M_6)	OUT	"		51	U
H	" M_7	(M_7)	OUT	"		50	U
J	" M_8	(M_8)	OUT	"		49	U
K	" M_9	(M_9)	OUT	"	M REGISTER DIGITS	48	U
L	" M_{10}	(M_{10})	OUT	"		45	U
M	" M_{11}	(M_{11})	OUT	"		44	U
N	" M_{12}	(M_{12})	OUT	"		43	U
P	" M_{13}	(M_{13})	OUT	"		42	U
R	" M_{14}	(M_{14})	OUT	"		41	U
S	" M_{15}	(M_{15})	OUT	"		40	U
T	" M_{16}	(M_{16})	OUT	"		39	U
U	" M_{17}	(M_{17})	OUT	"		38	U
V	" M_{18}	(M_{18})	OUT	"		37	U

SOCKET SKT 2 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
W	MONITOR J_1	(J_1)	OUT	NOTE 2	J REGISTER (STORE ADDRESS)	56	S
X	" J_2	(J_2)	OUT	"		55	S
Y	" J_3	(J_3)	OUT	"		54	S
Z	" J_4	(J_4)	OUT	"		53	S
a	" J_5	(J_5)	OUT	"		52	S
b	" J_6	(J_6)	OUT	"		51	S
c	" J_7	(J_7)	OUT	"		50	S
d	" J_8	(J_8)	OUT	"		49	S
e	" J_9	(J_9)	OUT	"		48	S
f	" J_{10}	(J_{10})	OUT	"		45	S
g	" J_{11}	(J_{11})	OUT	"		44	S
h	" J_{12}	(J_{12})	OUT	"		43	S
i	" J_{13}	(J_{13})	OUT	"		42	S
j	" J_{14}	(J_{14})	OUT	"		41	S
k	" J_{15}	(J_{15})	OUT	"		40	S
m	" J_{16}	(J_{16})	OUT	"		39	S

SOCKET SKT 2 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
n	MONITOR P_1	(P_1)	OUT	NOTE 1	PERIPHERAL ADDRESS	56	Y
p	" P_2	(P_2)	OUT	"		55	Y
q	" P_3	(P_3)	OUT	"		54	Y
r	" P_4	(P_4)	OUT	"		53	Y
s	" P_5	(P_5)	OUT	"		52	Y
t	" P_6	(P_6)	OUT	"		51	Y
u	" P_7	(P_7)	OUT	"		50	Y
v	" P_8	(P_8)	OUT	"		49	Y
w	" P_9	(P_9)	OUT	"		48	Y
x	" P_{10}	(P_{10})	OUT	"		45	Y
y	" P_{11}	(P_{11})	OUT	"		44	Y
z	" PC_1	(PC_1)	OUT	"		23	P
AA	" PC_2	(PC_2)	OUT	"		23	K
BB	" PC_3	(PC_3)	OUT	"	PROCESS COUNTER	23	V
CC	" PC_4	(PC_4)	OUT	"		23	Y
DD	" PC_5	(PC_5)	OUT	"		24	P
EE	" PC_6	(PC_6)	OUT	"		24	K
FF	" PC_7	(PC_7)	OUT	"		24	V

SOCKET SKT 2 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
GG	MONITOR PC_8	(PC_8)	OUT	NOTE 1	PROCESS COUNTER	24	Y
HH	" PC_9	(PC_9)	OUT	"		25	P
JJ	" PC_{10}	(PC_{10})	OUT	"		25	K
KK	" PC_{11}	(PC_{11})	OUT	"		25	V
LL	" PC_{12}	(PC_{12})	OUT	"		25	Y
MM	COMPUTER 0V		OUT	NOTE 9		31	A
NN	" + 6V			No connection in computer, voltage rails are wired through display from SKT 1			
PP	" - 6V						

SOCKET SKT 3 DEF. 5325/3 TYPE: THORNE PT00E 24-61 SY (Computer to Display Unit)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 24-61 PY

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH				CABLE SCREEN	Chassis	Bolt Tag
B	MONITOR F_1	(F_1)	OUT		F-UNIT DIGITS (BROUGHT OUT TO SKT. 3 BUT NOT MONITORED BY DISPLAY UNIT)	56	K
C	" F_2	(F_2)	OUT			55	K
D	" F_3	(F_3)	OUT			54	K
E	" F_4	(F_4)	OUT			53	K
F	" F_5	(F_5)	OUT			52	K
G	" F_6	(F_6)	OUT			51	K
H	" F_7	(F_7)	OUT			50	K
J	" F_8	(F_8)	OUT			49	K
K	" F_9	(F_9)	OUT			48	K
L	" F_{10}	(F_{10})	OUT			45	K
M	" F_{11}	(F_{11})	OUT			44	K
N	" F_{12}	(F_{12})	OUT			43	K
P	" F_{13}	(F_{13})	OUT			42	K
R	" F_{14}	(F_{14})	OUT			41	K
S	" F_{15}	(F_{15})	OUT			40	K
T	" F_{16}	(F_{16})	OUT			39	K
U	" F_{17}	(F_{17})	OUT			38	K
V	" F_{18}	(F_{18})	OUT			37	K

SOCKET SKT 3 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
W	MONITOR C_1	(C_1)	OUT		CARRY DIGITS (BROUGHT OUT TO SKT 3 BUT NOT MONITORED BY DISPLAY UNIT)	56	F
X	" C_2	(C_2)	OUT			55	F
Y	" C_3	(C_3)	OUT			54	F
Z	" C_4	(C_4)	OUT			53	F
a	" C_5	(C_5)	OUT			52	F
b	" C_6	(C_6)	OUT			51	F
c	" C_7	(C_7)	OUT			50	F
d	" C_8	(C_8)	OUT			49	F
e	" C_9	(C_9)	OUT			48	F
f	" C_{10}	(C_{10})	OUT			45	F
g	" C_{11}	(C_{11})	OUT			44	F
h	" C_{12}	(C_{12})	OUT			43	F
i	" C_{13}	(C_{13})	OUT			42	F
j	" C_{14}	(C_{14})	OUT			41	F
k	" C_{15}	(C_{15})	OUT			40	F
m	" C_{16}	(C_{16})	OUT			39	F
n	" C_{17}	(C_{17})	OUT			38	F
p	" C_{18}	(C_{18})	OUT			37	F

SOCKET SKT 3 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
q	MONITOR FUNCTION DRIVE	(FD)	OUT	NOTE 1		6	S
r	MONITOR I_1	(I_1)	OUT	"		41	Y
s	" I_2	(I_2)	OUT	"	I REGISTER DIGITS	40	Y
t	" I_3	(I_3)	OUT	"		39	Y
u	" I_4	(I_4)	OUT	"		38	Y
v	" AA1'	(AA1')	OUT	"		21	K
w	" AA2'	(AA2')	OUT	"	CURRENT CYCLE ADDRESS	21	U
x	" AA3'	(AA3')	OUT	"		21	AF
y	SPARE		OUT	"			
z	MONITOR AA1	(AA1)	OUT	"		21	M
AA	" AA2	(AA2)	OUT	"	NEXT CYCLE ADDRESS	21	X
BB	" AA3	(AA3)	OUT	"		21	AA
CC	SPARE						
DD	MONITOR CA	(CA)	OUT	"		7	Z
EE	" CB	(CB)	OUT	"	CONDITIONALS A & B	7	V
FF	" C	(C)	OUT	"	MATRIX CONTROL	6	N

SOCKET SKT 3 (Contd) (Computer to Display Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
GG	MONITOR CD	(CD)	OUT	NOTE 1	CONDITIONAL D	6	V
HH	" RESET	(RESET)	OUT	"		2	Z
JJ	" STOP	(STOP)	OUT	"		2	T
KK	" NOT READY	(NOT RDY.)	OUT	"	COMPUTER NOT READY	2	AC
LL	" TEMP. LOW	(TEMP. LOW)	OUT	"	COMPUTER UNDER TEM.	65	AE
MM	COMPUTER +6V		OUT	Linked to PL6 pins	G, H, J, K	31	B
NN	" -6V		OUT	" " " "	L, M	31	AK
PP	" 0V		OUT	NOTE 9		31	1

SOCKET SKT 4 DEF. 5325/3 TYPE: THORNE PT00E 26-61 S (Computer I/P, O/P)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06W 24-61 P

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	COMPUTER 0V		OUT	NOTE 9	CABLE SCREEN	BUS BAR	
B	OUTPUT A REGISTER BIT 1	OA_1	OUT	NOTE 3		31	3
C	" A " " 2	OA_2	OUT	"		31	4
D	" A " " 3	OA_3	OUT	"		31	5
E	" A " " 4	OA_4	OUT	"		31	6
F	" A " " 5	OA_5	OUT	"		31	7
G	" A " " 6	OA_6	OUT	"		31	8
H	" A " " 7	OA_7	OUT	"		31	9
J	" A " " 8	OA_8	OUT	"	DATA OUTPUT TO SELECT PERIPHERALS FROM REGISTER A.	31	10
K	" A " " 9	OA_9	OUT	"		31	11
L	" A " " 10	OA_{10}	OUT	"		31	12
M	" A " " 11	OA_{11}	OUT	"		31	13
N	" A " " 12	OA_{12}	OUT	"		31	14
P	" A " " 13	OA_{13}	OUT	"		31	15
R	" A " " 14	OA_{14}	OUT	"		31	16
S	" A " " 15	OA_{15}	OUT	"		31	17
T	" A " " 16	OA_{16}	OUT	"		31	18
U	" A " " 17	OA_{17}	OUT	"		31	19
V	" A " " 18	OA_{18}	OUT	"		31	20

SOCKET SKT 4 (Contd) (Computer I/P, O/P)

PIN REF	WAVEFORM TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
W	O/P SELECT ADDRESS BIT 1	OS_1	OUT	NOTE 3		32	3
X	" " " 2	OS_2	OUT	"		32	4
Y	" " " 3	OS_3	OUT	"		32	5
Z	" " " 4	OS_4	OUT	"		32	6
a	" " " 5	OS_5	OUT	"		32	7
b	" " " 6	OS_6	OUT	"	PERIPHERAL ADDRESS BITS	32	8
c	" " " 7	OS_7	OUT	"		32	9
d	" " " 8	OS_8	OUT	"		32	10
e	" " " 9	OS_9	OUT	"		32	11
f	" " " 10	OS_{10}	OUT	"		32	12
g	" " " 11	OS_{11}	OUT	"		32	13
h	SPARE						
i	SPARE						
j	SPARE						
k	SPARE						
m	SPARE						
n	SPARE						
p	COMPUTER ON (+ 6V)		OUT	NOTE 10		17	B

SOCKET SKT 4 (Contd) (Computer I/P, O/P)

PIN REF	WAVEFORM TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
q	INPUT G REGISTER BIT 1	IG_1	IN	NOTE 4	DATA INPUT FROM SELECTED PERIPHERALS TO G REGISTER	28	C
r	" G " " 2	IG_2	IN	"		28	D
s	" G " " 3	IG_3	IN	"		28	E
t	" G " " 4	IG_4	IN	"		28	F
u	" G " " 5	IG_5	IN	"		28	H
v	" G " " 6	IG_6	IN	"		28	J
w	" G " " 7	IG_7	IN	"		28	K
x	" G " " 8	IG_8	IN	"		28	L
y	" G " " 9	IG_9	IN	"		28	M
z	" G " " 10	IG_{10}	IN	"		28	R
AA	" G " " 11	IG_{11}	IN	"		28	S
BB	" G " " 12	IG_{12}	IN	"		28	T
CC	" G " " 13	IG_{13}	IN	"		28	U
DD	" G " " 14	IG_{14}	IN	"		28	V
EE	" G " " 15	IG_{15}	IN	"		28	W
FF	" G " " 16	IG_{16}	IN	"		28	AB
GG	" G " " 17	IG_{17}	IN	"		28	AC
HH	" G " " 18	IG_{18}	IN	"		28	AD

SOCKET SKT 4 (Contd) (Computer I/P, O/P)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
JJ	SPARE						
KK	SPARE						
LL	MAINS EARTH					Chassis	Bolt Tag
MM	SPARE						
NN	SPARE						
PP	RESET		OUT	NOTE 3		32	20

SOCKET SKT 5 DEF. 5325/3 TYPE: THORNE PT00E 20-41S (Computer to Control Unit)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 20-41P

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH				CABLE SCREEN	Chassis	Bolt Tag
B	POWER ON		OUT	Linked to PL6 pin X		PL6	PIN X
C	POWER CONTROL IN		IN	" " PL6 pin Z		PL6	PIN Z
D	TEST (BAR)	$(TEST_k)$				1	5
E	POWER OFF		OUT	" " PL6 pin Y		PL6	PIN Y
F	SPARE						
G	SPARE						
H	MONITOR RESET	$(RESET)_1$	OUT	NOTE 1		2	U
J	SPARE						
K	SPARE						
L	POWER OFF LAMP + VE 24V		OUT	Linked to PL6 pin a		PL6	PIN a
M	POWER OFF LAMP - VE 24V		OUT	" " PL6 pin b		PL6	PIN b
N	SPARE						
P	STOP KEY (BAR)	$\overline{STOP_k}$	IN	NOTE 5		1	25
R	MONITOR STOP	$(STOP)_2$	OUT	NOTE 1		2	E
S	SPARE						
T	RESTART KEY	$RESTART_k$	IN	NOTE 5		1	C
U	RESTART KEY (BAR)	$\overline{RESTART_k}$	IN	"		1	3
V	JUMP KEY	$JUMP_k$	IN	"		1	M

SOCKET SKT 5 (Contd) (Computer to Control Unit)

	WAVEFORM					INTERNAL CONNECTION	
PIN REF	TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	BOARD POSN.	PIN
W	JUMP KEY (BAR)	$\overline{JUMP_k}$	IN	NOTE 5		1	11
X	MONITOR LEVEL 1 ACTIVE	(ACTIVE 1)	OUT	NOTE 1		1	Y
Y	MONITOR LEVEL 1 INTERRUPT	(INT 1)	OUT	"		3	F
Z	MONITOR LEVEL 2 ACTIVE	(ACTIVE 2)	OUT	"		1	V
a	MONITOR LEVEL 2 INTERRUPT	(INT 2)	OUT	"		3	W
b	CONTINUOUS NIMBER GENERATOR	$CINS_k$	IN	NOTE 5		1	J
c	CONTINUOUS NUMBER GENERATOR (BAR)	$\overline{CINS_k}$	IN	"		1	8
d	CYCLE REPEAT KEY (BAR)	$\overline{TCS_k}$	IN	"		1	AB
e	CYCLE STOP KEY (BAR)	$\overline{CS_k}$	IN	"		1	H
f	ORDER STOP KEY (BAR)	$\overline{OS_k}$	IN	"		1	19
g	MONITOR LEVEL 3 ACTIVE	(ACTIVE 3)	OUT	NOTE 1		1	S
h	MONITOR LEVEL 3 INTERRUPT	(INT 3)	OUT	NOTE 1		3	AD
i	STOP MODE NORMAL KEY (BAR)	$\overline{SMN_k}$	IN	NOTE 5		4	7
j	SPARE						
k	AUTO KEY	$AUTO_k$	IN	"		1	L
m	SPARE						
n	SPARE						

SOCKET SKT 5 (Contd) (Computer to Control Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
p	AUDIO INNER	(SCREENING)	OUT	NOTE 3	CO-AXIAL	32	14
q	AUDIO OUTER	Computer 0V	OUT	NOTE 9	CO-AXIAL		
r	COMPUTER 0V		OUT	"		30	1
s	COMPUTER + 6V		OUT	NOTE 10		31	2
t	COMPUTER - 6V		OUT	"		31	31

PLUG PL6 DEF. 5325/3 TYPE: THORNE PT00E 24-61P (Computer to Power Supply)
MATING FREE SOCKET DEF. 5325/3 TYPE: THORNE PT06E 24-61S

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH			NOTE 9	CABLE SCREEN	Chassis	Bolt Tag
B	COMPUTER 0V			"		1	1
C	COMPUTER 0V			"		4	1
D	COMPUTER 0V			"		8	1
E	COMPUTER 0V			"		12	1
F	COMPUTER 0V MAINS SUPPLY			"		20	A
G	COMPUTER +6V INTO COMP.			NOTE 10		1	2
H	COMPUTER + 6V			"		32	B
J	COMPUTER + 6V			"		33	2
K	COMPUTER + 6V			"		57	B
L	COMPUTER - 6V			"		1	31
M	COMPUTER - 6V			"		33	31
N	VARIABLE SUPPLY + VE			NOTE 14	COMPUTER 0V	65	C
P	VARIABLE SUPPLY - VE		IN	"		65	1
R	TEMP. DEPENDENT REFERENCE VOLTAGE		OUT	NOTE 6		65	6
S	COMPUTER - 16V			NOTE 15		59	AJ
T	POWER SUPPLY CORRECT (BAR)	$\overline{\text{PSC}}$	IN	NOTE 3		59	AE
U	LOGIC 0V			NOTE 9		1	A

PLUG PL6 (Contd) (Computer to Power Supplies)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
V	+24V		IN	NOTE 17	RELAY SUPPLY	+ 24V TAG	
W	- 24V					- 24V TAG	
X	POWER ON	0V		Linked to SKT 5 pin	B	SKT 5	PIN B
Y	POWER OFF		IN	" " " "	E	SKT 5	PIN E
Z	POWER CONTROL IN	0V		" " " "	C	SKT 5	PIN C
a	POWER OFF LAMP + VE + 24V		IN	" " " "	L	SKT 5	PIN L
b	POWER OFF LAMP - VE - 24V		IN	" " " "	M	SKT 5	PIN M
c	SPARE						
d	COMPUTER 0V			NOTE 9		24	A
e	COMPUTER 0V		IN	"		28	A
f	COMPUTER 0V			"		32	A
g	COMPUTER + 6V			NOTE 10		64	1
h	COMPUTER + 6V		IN	"		64	40
i	COMPUTER + 6V					65	2
j	COMPUTER + 6V			"		66	40
k	COMPUTER - 6V		IN	NOTE 10		59	A
m	COMPUTER - 6V		IN	"		66	A
n	+ 6V SENSE WIRE		OUT	"		1	B
p	- 6V SENSE WIRE		OUT	"		1	AK

PLUG PL6 (Contd) (Computer to Power Supplies)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
q	SPARE						
r	- 16V SENSE WIRE		IN	NOTE 5		59	30
s	POWER SUPPLY MARGINS		IN	Linked to SKT 7 pin	D	SKT 7	PIN D
t			OUT	" " " "	C	SKT 7	PIN C
u			IN	" " " "	B	SKT 7	PIN B
v	SPARE						
w	SPARE						
x	VARIABLE SUPPLY MARGINS		OUT	" " " "	F	SKT 7	PIN F
y	AUTOSTART/MANUAL		OUT	Linked to SKT 11 pin	R	SKT 11	PIN r
z	OVER TEMPERATURE		OUT	NOTE 3		65	10
AA	MARGIN TEST INHIBIT		IN	Linked to SKT 7 pin	M	SKT 7	PIN M
BB	MAIN INVERTER ON/OFF TEST LINK		IN	LINKED			
CC			OUT				
DD	INPUT VOLTAGE SENSE TEST LINK		IN	LINKED			
EE			OUT				
FF	OUTPUT VOLTAGE SENSE TEST LINK		IN	LINKED			
GG			OUT				
HH	SPARE						

PLUG PL6 (Contd) (Computer to Power Supplies)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
JJ	SPARE						
KK	SPARE						
LL	SPARE						
MM	SPARE						
NN	SPARE						
PP	SPARE						

SOCKET SKT 7 DEF. 5325/3 TYPE: THORNE PT00E 18-32S (Computer to Marginal Test Unit)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 18-32P

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH				CABLE SCREEN	Chassis	Bolt Tag
B			OUT	Linked to PL6 pin u		PL6	PIN u
C	POWER SUPPLY MARGINS		IN	" " " " t	AUXILIARY -6V	PL6	PIN t
D			OUT	" " " " s		PL6	PIN s
E	VARIABLE		OUT	" " " " R	TEMP. DEPENDENT	59	5
F	SUPPLY MARGINS		IN	" " " " x	REFERENCE VOLTS	PL6	PIN x
G			OUT	NOTE 9	COMPUTER 0V	29	A
H	DRIVE CURRENT MARGINS		IN	NOTE 11		59	6
J	MAIN TIMING LOOP MARGINS		OUT	NOTE 10		30	B
K			IN	NOTE 12		4	3
L	PULSE GENERATOR MARGINS		IN	NOTE 13		25	12
M	MARGIN TEST INHIBIT		OUT	Connected to PL6 pin AA		PL6	PIN AA
N	SPARE						
P	SPARE						
R	SPARE						
S	SPARE						
T	SPARE						
U	SPARE						

SOCKET SKT 7 (Contd) (Computer to Marginal Test Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
V	SPARE						
W	SPARE						
X	SPARE						
Y	SPARE						
Z	SPARE						
a	SPARE						
b	SPARE						
c	SPARE						
d	SPARE						
e	SPARE						
f	SPARE						
g	SPARE						
h	SPARE						
j	SPARE						

SOCKET SKT 8 DEF. 5325/3 TYPE: THORNE PT00E 18-32SX (Extra Store)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 18-32PX

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	O/P OF M-REGISTER BIT 1	M_{1-x}	OUT	NOTE 7	COAXIAL INNER	27	C
B	" " " "	0V			" SCREEN	0V BUS-BAR	
C	" " " " 2	M_{2-x}	OUT	"	" INNER	27	D
D	" " " "	0V			" SCREEN	0V BUS-BAR	
E	" " " " 3	M_{3-x}	OUT	"	" INNER	27	E
F	" " " "	0V			" SCREEN	0V BUS-BAR	
G	" " " " 4	M_{4-x}	OUT	"	" INNER	27	F
H	" " " "	0V			" SCREEN	0V BUS-BAR	
J	" " " " 5	M_{5-x}	OUT	"	" INNER	27	H
K	" " " "	0V			" SCREEN	0V BUS-BAR	
L	" " " " 6	M_{6-x}	OUT	"	" INNER	27	J
M	" " " "	0V			" SCREEN	0V BUS-BAR	
N	" " " " 7	M_{7-x}	OUT	"	" INNER	27	K
P	" " " "	0V			" SCREEN	0V BUS-BAR	
R	" " " " 8	M_{8-x}	OUT	"	" INNER	27	L
S	" " " "	0V			" SCREEN	0V BUS-BAR	
T	" " " " 9	M_{9-x}	OUT	"	" INNER	27	M
U	" " " "	0V			" SCREEN	0V BUS-BAR	

SOCKET SKT 8 (Contd) (Extra Store)

PIN REF	WAVEFORM TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
V	O/P OF M-REGISTER BIT 10	M_{10-x}	OUT	NOTE 7	COAXIAL INNER	27	N
W	" " " "	0V			" SCREEN	0V BUS-BAR	
X	" " " " 11	M_{11-x}	OUT	"	" INNER	27	P
Y	" " " "	0V			" SCREEN	0V BUS-BAR	
Z	" " " " 12	M_{12-x}	OUT	"	" INNER	27	R
a	" " " "	0V			" SCREEN	0V BUS-BAR	
b	" " " " 13	M_{13-x}	OUT	"	" INNER	27	S
c	" " " "	0V			" SCREEN	0V BUS-BAR	
d	" " " " 14	M_{14-x}	OUT	"	" INNER	27	T
e	" " " "	0V			" SCREEN	0V BUS-BAR	
f	" " " " 15	M_{15-x}	OUT	"	" INNER	27	U
g	" " " "	0V			" SCREEN	0V BUS-BAR	
h	" " " " 16	M_{16-x}	OUT	"	" INNER	27	V
j	" " " "	0V			" SCREEN	0V BUS-BAR	

SOCKET SKT 9 DEF. 5325/3 TYPE: THORNE PT00E 18-32SY (Extra Store)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 18-32PY

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	J-REGISTER BIT 1	J_{1-x}	OUT	NOTE 7	COAXIAL INNER	27	Y
B	" "	0V			" SCREEN	0V BUS-BAR	
C	" " 2	J_{2-x}	OUT	"	" INNER	27	Z
D	" "	0V			" SCREEN	0V BUS-BAR	
E	" " 3	J_{3-x}	OUT	"	" INNER	27	AA
F	" "	0V			" SCREEN	0V BUS-BAR	
G	" " 4	J_{4-x}	OUT	"	" INNER	27	AB
H	" "	0V			" SCREEN	0V BUS-BAR	
J	" " 5	J_{5-x}	OUT	"	" INNER	27	AC
K	" "	0V			" SCREEN	0V BUS-BAR	
L	" " 6	J_{6-x}	OUT	"	" INNER	27	AD
M	" "	0V			" SCREEN	0V BUS-BAR	
N	" " 7	J_{7-x}	OUT	"	" INNER	27	AE
P	" "	0V			" SCREEN	0V BUS-BAR	
R	" " 8	J_{8-x}	OUT	"	" INNER	27	AF
S	" "	0V			" SCREEN	0V BUS-BAR	
T	" " 9	J_{9-x}	OUT	"	" INNER	27	AH
U	" "	0V			" SCREEN	0V BUS-BAR	

SOCKET SKT 9 (Contd) (Extra Store)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
V	J-REGISTER BIT 10	J_{10-x}	OUT	NOTE 7	COAXIAL INNER	27	AJ
W	" "	0V			" SCREEN	0V BUS-BAR	
X	" " 11	J_{11-x}	OUT	"	" INNER	26	26
Y	" "	0V			" SCREEN	0V BUS-BAR	
Z	" " 12	J_{12-x}	OUT	"	" INNER	26	25
a	" "	0V			" SCREEN	0V BUS-BAR	
b	" " 13	J_{13-x}	OUT	"	" INNER	26	22
c	" "	0V			" SCREEN	0V BUS-BAR	
d	" " 14	J_{14-x}	OUT	"	" INNER	26	21
e	" "	0V			" SCREEN	0V BUS-BAR	
f	" " 15	J_{15-x}	OUT	"	" INNER	26	18
g	" "	0V			" SCREEN	0V BUS-BAR	
h	" " 16	J_{16-x}	OUT	"	" INNER	26	14
j	" "	0V			" SCREEN	0V BUS-BAR	

SOCKET SKT 10 DEF. 5325/3 TYPE: THORNE PT00E 18-32SW (Computer to Paper Tape Controller)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 18-32PW

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	READER CODE 1	IR_1	IN	NOTE 3		29	C
B	" " 2	IR_2	IN	"		29	D
C	" " 3	IR_3	IN	"		29	E
D	" " 4	IR_4	IN	"		29	F
E	" " 5	IR_5	IN	"		29	L
F	" " 6	IR_6	IN	"		29	H
G	" " 7	IR_7	IN	"		29	J
H	" " 8	IR_8	IN	"		29	K
J	PUNCH CODE 1	OP_1	OUT	"		31	21
K	" " 2	OP_2	OUT	"		31	22
L	" " 3	OP_3	OUT	"		31	23
M	" " 4	OP_4	OUT	"		31	24
N	" " 5	OP_5	QUT	"		31	25
P	" " 6	OP_6	OUT	"		31	26
R	" " 7	OP_7	OUT	"		31	27
S	" " 8	OP_8	OUT	"		31	28
T	MAINS EARTH					Chassis	Bolt Tag
U	ADDRESS BIT 3	P_3	OUT	"		32	18
V	READERS SELECT	STR	OUT	"	COAXIAL INNER	30	14

SOCKET SKT 10 (Contd) (Computer to Paper Tape Controller)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
W	READER REPLY	RTR	IN	NOTE 3	COAXIAL INNER	30	D
X	ADDRESS BIT 1	P_1	OUT	"		32	17
Y	ADDRESS BIT 2	P_2	OUT	"		32	15
Z	AUTOLINK	0V		NOTE 9	CONNECTED TO SKT 11 pin Z	SKT 11	Z
a	PUNCH INTERRUPT		IN	Connected to SKT 13 pin T	COAXIAL INNER	SKT 13	PIN T
b	ADDRESS BIT 4	P_4	OUT	NOTE 3		32	19
c	READER INTERRUPT		IN	Connected to SKT 13 pin V		SKT 13	PIN V
d	COMPUTER RESET		OUT	NOTE 3		32	16
e	COMPUTER 0V		OUT	NOTE 9		27	1
f	+ 24V		OUT	NOTE 17	RELAY SUPPLIES	+ 24V TAG	
g	- 24V		OUT	NOTE 17		- 24V TAG	
h	PUNCH SELECT	STP	OUT	NOTE 3	COAXIAL INNER	30	15
j	PUNCH REPLY	RTP	IN	"	" "	30	C

SOCKET SKT 11 DEF. 5325/3 TYPE: THORNE PT00E 20-41 SW (Computer to Control Unit)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 20-41 PW

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	MAINS EARTH				CABLE SCREEN	Chassis	Bolt Tag
B	NUMBER GEN- KEY BIT 1	$NG1_k$	IN	NOTE 5		56	18
C	" " " " 2(BAR)	$\overline{NG2}_k$	IN	"		29	U
D	" " " " 3(BAR)	$\overline{NG3}_k$	IN	"		29	T
E	" " " " 4(BAR)	$\overline{NG4}_k$	IN	"		29	S
F	" " " " 5	$NG5_k$	IN	"		52	18
G	" " " " 6	$NG6_k$	IN	"		51	18
H	" " " " 7	$NG7_k$	IN	"		50	18
J	" " " " 8	$NG8_k$	IN	"		49	18
K	" " " " 9	$NG9_k$	IN	"		48	18
L	" " " " 10	$NG10_k$	IN	"		45	18
M	" " " " 11	$NG11_k$	IN	"		44	18
N	" " " " 12	$NG12_k$	IN	"		43	18
P	" " " " 13	$NG13_k$	IN	"		42	18
R	" " " " 14(BAR)	$\overline{NG14}_k$	IN	"		29	P
S	" " " " 15(BAR)	$\overline{NG15}_k$	IN	"		29	V
T	" " " " 16(BAR)	$\overline{NG16}_k$	IN	"		29	N
U	" " " " 17(BAR)	$\overline{NG17}_k$	IN	"		1	17
V	" " " " 18(BAR)	$\overline{NG18}_k$	IN	"		29	R

SOCKET SKT 11 (Contd) (Computer to Control Unit)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
W	INTERRUPT LEVEL 1		IN	NOTE 4		3	9
X	" " 2		IN	"		3	10
Y	" " 3		IN	"		3	11
Z	AUTOLINK		IN	0V with paper tape station connected	CONNECTED TO SKT 10 PIN Z	SKT 10	PIN Z
a	SPARE				a) may be used for OVER/) UNDER	59	5
b	SPARE				b) TEMPERATURE WARN-) ING thermostats		
c	SPARE						
d	SPARE						
e	COMPUTER 0V		IN	NOTE 9		26	A
f	OBEY NUMBER GEN. KEY	ONG_k	IN	NOTE 5		1	7
g	OBEY NUMBER GEN. KEY(BAR)	$\overline{ONG}_k$	IN	"		1	F
h	ENTER NUMBER GEN. KEY	ENG_k	IN	"		1	6
i	ENTER NUMBER GEN. KEY(BAR)	$\overline{ENG}_k$	IN	"		1	4
j	RESET KEY	$RESET_k$	IN	"		1	24
k	SPARE						
m	PERIPHERAL SUPPRESS LEVEL 1	PS_1	IN	NOTE 4		3	E
n	" " " 2	PS_2	IN	"		3	L
p	" " " 3	PS_3	IN	"		3	S

SOCKET SKT 11 (Contd) (Computer to Control Unit)

	WAVEFORM					INTERNAL CONNECTION	
PIN REF	TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	BOARD POSN.	PIN
q	NUMBER GEN. KEY BIT 17	$NG17_k$	IN	NOTE 7		1	18
r, s	AUTO START LINK			Linked to PL6 pin y	LINKED ON INSERTION START ADDRESS PLUG	PL6	PIN y
				NOTE 9		26	1
t	COMPUTER + 6V		OUT	NOTE 10		30	2

SOCKET SKT 13 DEF. 5325/3 TYPE: THORNE PT00E 14-19S (Computer I/P, O/P)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06W 14-19P

	WAVEFORM					INTERNAL CONNECTION	
PIN REF	TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	BOARD POSN.	PIN
A	PERIPHERAL INT. LEVEL 1	PI_1	IN	NOTE 4	COAXIAL INNER	29	AE
B	0V		IN	NOTE 9	" SCREEN	0V BUS-BAR	
C	PERIPHERAL INT. LEVEL 2	PI_2	IN	NOTE 4	" INNER	29	AF
D	0V		IN	NOTE 9	" SCREEN	0V BUS-BAR	
E	PERIPHERAL INT. LEVEL 3	PI_3	IN	NOTE 4	" INNER	29	AH
F	0V		IN	NOTE 9	" SCREEN	0V BUS-BAR	
G	SELECT O/P PERIPHERAL	SOP	OUT	NOTE 8	" INNER	30	20
H	0V		OUT	NOTE 9	" SCREEN	0V BUS-BAR	
J	SELECT I/P PERIPHERAL	SIP	OUT	NOTE 8	" INNER	30	21
K	0V		OUT	NOTE 9	" SCREEN	0V BUS-BAR	
L	PERIPHERAL REPLY I/P, O/P	PR	IN	NOTE 4	" INNER	30	E
M	0V		IN	NOTE 9	" SCREEN	0V BUS-BAR	
N	BLOCK TRANSFER	BT	OUT	NOTE 8	" INNER	30	U
P	0V		OUT	NOTE 9	" SCREEN	0V BUS-BAR	
R	LAST WORD	LW	OUT	NOTE 8	" INNER	30	13
S	0V		OUT	NOTE 9	" SCREEN	0V BUS-BAR	
T	PUNCH INTERRUPT		IN	Linked to SKT 10 pin a	" INNER	SKT 10	a
U	0V		IN	NOTE 9 shared with pin T and V. Linked to SKT 10 pin e	" SCREEN	SKT 10	e
V	READER INTERRUPT		IN	Linked to SKT 10 pin c	" INNER	SKT 10	c

SOCKET SKT 14 DEF. 5325/3 TYPE: THORNE PT00E 24-61SZ (Computer to Extra Store)
MATING FREE PLUG DEF. 5325/3 TYPE: THORNE PT06E 24-61PZ

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
A	OUTPUT M-REGISTER BIT 17	M.17-x	OUT	NOTE 7	COAXIAL INNER	27	W
B	" " " "	0V	OUT		" SCREEN	0V BUS-BAR	
C	" " " 18	M.18-x	OUT	"	" INNER	27	X
D	" " " "	0V	OUT		" SCREEN	0V BUS-BAR	
E	EXTERNAL STORE O/P BIT 1	$STORE_{1-x}$	IN	"	" INNER	26	E
F	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
G	EXTERNAL STORE O/P BIT 2	$STORE_{2-x}$	IN	"	" INNER	26	D
H	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
J	EXTERNAL STORE O/P BIT 3	$STORE_{3-x}$	IN	"	" INNER	26	C
K	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
L	EXTERNAL STORE O/P BIT 4	$STORE_{4-x}$	IN	"	" INNER	26	L
M	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
N	EXTERNAL STORE O/P BIT 5	$STORE_{5-x}$	IN	"	" INNER	26	K
P	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
R	EXTERNAL STORE O/P BIT 6	$STORE_{6-x}$	IN	"	" INNER	26	J
S	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
T	EXTERNAL STORE O/P BIT 7	$STORE_{7-x}$	IN	"	" INNER	26	T
U	" " " "	0V	IN		" SCREEN	0V BUS-BAR	

SOCKET SKT 14 (Contd) (Computer to Extra Store)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/ OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
V	EXTERNAL STORE O/P BIT 8	$STORE_{8-x}$	IN	NOTE 7	COAXIAL INNER	26	S
W	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
X	EXTERNAL STORE O/P BIT 9	$STORE_{9-x}$	IN	"	" INNER	26	R
Y	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
Z	EXTERNAL STORE O/P BIT 10	$STORE_{10-x}$	IN	"	" INNER	26	Y
a	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
b	EXTERNAL STORE O/P BIT 11	$STORE_{11-x}$	IN	"	" INNER	26	W
c	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
d	EXTERNAL STORE O/P BIT 12	$STORE_{12-x}$	IN	"	" INNER	26	V
e	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
f	EXTERNAL STORE O/P BIT 13	$STORE_{13-x}$	IN	"	" INNER	26	AA
g	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
h	EXTERNAL STORE O/P BIT 14	$STORE_{14-x}$	IN	"	" INNER	26	AC
i	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
j	EXTERNAL STORE O/P BIT 15	$STORE_{15-x}$	IN	"	" INNER	26	AE
k	" " " "	0V	IN		SCREEN	0V BUS-BAR	
m	EXTERNAL STORE O/P BIT 16	$STORE_{16-x}$	IN	"	" INNER	26	AJ
n	" " " "	0V	IN		" SCREEN	0V BUS-BAR	

SOCKET SKT 14 (Contd) (Computer to Extra Store)

PIN REF	WAVEFORM TITLE	WAVEFORM ABBREV.	IN/OUT	TOLERANCES	NOTES	INTERNAL CONNECTION BOARD POSN.	INTERNAL CONNECTION PIN
p	EXTERNAL STORE O/P BIT 17	$STORE_{17-x}$	IN	NOTE 7	COAXIAL INNER	26	AH
q	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
r	EXTERNAL STORE O/P BIT 18	$STORE_{18-x}$	IN	"	" INNER	26	27
s	" " " "	0V	IN		" SCREEN	0V BUS-BAR	
t	TRIG READ (EXT)	TR_x	OUT	"	" INNER	26	11
u	" " "	0V	OUT		" SCREEN	0V BUS-BAR	
v	TRIG WRITE (EXT)	TW_x	OUT	"	" INNER	26	10
w	" " "	0V	OUT		" SCREEN	0V BUS-BAR	
x	READ GATE STROBE	RGS	IN	"	" INNER	29	AA
y	" " "	0V	IN		" SCREEN	0V BUS-BAR	
z	WRITE GATE STROBE	WGS	IN	"	" INNER	29	Z
AA	" " "	0V	IN		" SCREEN	0V BUS-BAR	
BB	POWER SUPPLY CORRECT	PSC_x	IN	"	" INNER	2	29
CC	" " "	0V	IN		" SCREEN	0V BUS-BAR	
DD	STORE STROBE INHIBIT	SSI_x	OUT	"	" INNER	26	6
EE	" " "	0V	OUT		" SCREEN	0V BUS-BAR	
FF	RESET	$RESET_x$	OUT	"	" INNER	26	5
GG	"	0V	OUT		" SCREEN	0V BUS-BAR	

SOCKET SKT 14 (Contd) (Computer to Extra Store)

	WAVEFORM					INTERNAL CONNECTION	
PIN REF	TITLE	ABBREV.	IN/ OUT	TOLERANCES	NOTES	BOARD POSN.	PIN
HH	+ 24V		OUT	NOTE 17		+ 24V TAG	
JJ	MAINS EARTH		OUT	"		Chassis	Bolt Tag
KK	- 24V		OUT	"		- 24V TAG	
LL	SPARE				) May be used for OVER/		
MM	SPARE				) UNDER TEMPERATURE		
NN	SPARE				) Warning thermostats		
PP	SPARE						